Datasheet

APM32A103CBT7

Arm® Cortex®-M3 based 32-bit MCU (Automotive grade)

Version: V1.2

1. Product characteristics

Core

- 32-bit Arm® Cortex®-M3 core
- Up to 96MHz working frequency

On-chip memory

- Flash：128KB
- SRAM：20KB

Clock

- HSECLK: 4~16MHz external crystal/ceramic oscillator supported
- LSECLK: 32.768KHz crystal/ceramic oscillator supported
- HSICLK: 8MHz RC oscillator calibrated by factory
- LSICLK: 40KHz RC oscillator supported
- PLL: Phase locked loop, 2~16 times of frequency supported

Reset and power management

- V_{DD} range: 2.0～3.6V
- V_{DDA} range: 2.0～3.6V
- V_{BAT} range of backup domain power supply: 1.8V～3.6V
- Power-on/power-down reset (POR/PDR) supported
- Programmable power supply voltage detector supported(PVD)

Low-power mode

- Sleep, stop and standby modes supported

DMA

- One 7-channel DMA

Debugging interface

- JTAG
- SWD

I/O

- Up to 37 I/Os
- All I/Os can be mapped to external interrup vector
- Up to 21 FT input I/Os

Communication peripherals

- 2 I2C interfaces (1Mbit/s), all of which support SMBus/PMBus
- 3 USART, support ISO7816, LIN and IrDA functions
- 2 SPI (18Mbps) interfaces
- 1 CAN
- 1 USBD

Analog peripherals

- 2 12-bit ADCs

Timer

- 1 16-bit advanced timers TMR1 that can provide 7-channel PWM output, support dead time generation and braking input functions
- 3 16-bit general-purpose timers TMR2/3/4, each with up to 4 independent channels to support input capture, output comparison, PWM, pulse count and other functions
- 2 watchdog timers: one independent watchdog IWDT and one window watchdog WWDT
- 1 24-bit autodecrement SysTick Timer

RTC

- Support calendar and clock functions

84Bytes backup register

CRC computing unit

FPU

- Independent FPU module supports floating point operations

96-bit unique device ID

Certification standards

- AEC-Q100-Rev-H Grade2

Contents

2. Product information

See the following table for APM32A103CBT7 product functions and peripheral configuration.

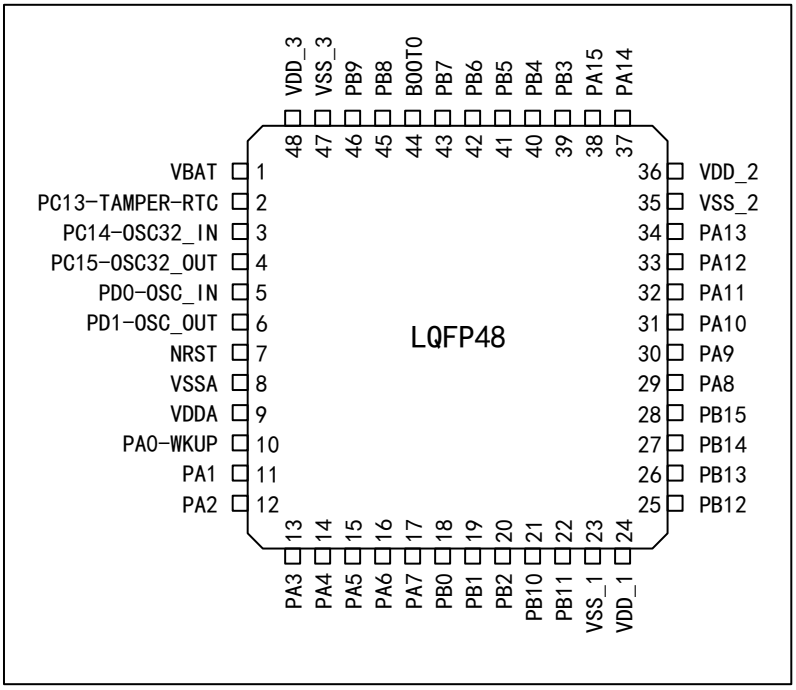
Table 1 Functions and Peripherals of APM32A103CBT7 Series Chips

Product		**APM32A103**
Model		CBT7
Package		LQFP48
Core and maximum working frequency		Arm® 32-bit Cortex®-M3@96MHz
Operating voltage		2.0~3.6V
Flash(KB)		128
SRAM(KB)		20
GPIOs		37
Communication interface	USART	3
	SPI	2
	I2C	2
	USBD	1
	CAN	1
Timer	16-bit advanced	1
	16-bit general	3
	System tick timer	1
	Watchdog	2
Real-time clock		1
12-bit ADC	Unit	2
	External channel	10
	Internal channel	1
FPU		1
Operating temperature		Ambient temperature:-40℃ to 105℃ Junction temperature:-40℃ to 125℃

3. Pin information

3.1. Pin distribution

Figure 1 Distribution Diagram of APM32A103CBT7 Series LQFP48 Pins



3.2. Pin function description

Table 2 Legends/Abbreviations Used in Output Pin Table

Name	Abbreviation	Definition
Pin name	Unless otherwise specified in parentheses below the pin name, the pin functions during and after reset are the same as the actual pin name	
Pin type	P	Power pin
	I	Only input pin
	I/O	I/O pin
I/O structure	5T	FT I/O
	5Tf	FT I/O, FM+ function
	STDA	I/O with 3.3 V tolerance, directly connected to ADC
	STD	I/O with 3.3 V tolerance
	B	Dedicated Boot0 pin
	RST	Bidirectional reset pin with built-in pull-up resistor
Note	Unless otherwise specified in the notes, all I/O is set as floating input during and after reset	

Name		Abbreviation	Definition
Pin function	Default multiplexing function	Function directly selected/enabled through peripheral register	
	Remap	Select this function through AFIO remapping register	

Table 3 Description of APM32A103CBT7 by Pin Number

Name (Function after reset)	Type	Structure	Default multiplexing function	Remap	LQFP48
V_{BAT}	P	-	-	-	1
PC13- TAMPER-RTC (PC13)	I/O	STD	TAMPER-RTC	-	2
PC14- OSC32_IN (PC14)	I/O	STD	OSC32_IN	-	3
PC15- OSC32_OUT (PC15)	I/O	STD	OSC32_OUT	-	4
OSC_IN	I	STD	-	PD0	5
OSC_OUT	O	STD	-	PD1	6
NRST	I/O	RST	-	-	7
V_{SSA}	P	-	-	-	8
V_{DDA}	P	-	-	-	9
PA0-WKUP (PA0)	I/O	STDA	WKUP/ USART2_CTS/ ADC12_IN0/ TMR2_CH1_ETR	-	10
PA1	I/O	STDA	USART2_RTS/ ADC12_IN1/ TMR2_CH2	-	11
PA2	I/O	STDA	USART2_TX/ ADC12_IN2/ TMR2_CH3	-	12
PA3	I/O	STDA	USART2_RX/ ADC12_IN3/ TMR2_CH4	-	13
PA4	I/O	STDA	SPI1_NSS/ USART2_CK/ ADC12_IN4	-	14
PA5	I/O	STDA	SPI1_SCK/ ADC12_IN5	-	15
PA6	I/O	STDA	SPI1_MISO/ ADC12_IN6/ TMR3_CH1	TMR1_BKIN	16

Name (Function after reset)	Type	Structure	Default multiplexing function	Remap	LQFP48
PA7	I/O	STDA	SPI1_MOSI/ ADC12_IN7/ TMR3_CH2	TMR1_CH1N	17
PB0	I/O	STDA	ADC12_IN8/ TMR3_CH3	TMR1_CH2N	18
PB1	I/O	STDA	ADC12_IN9/ TMR3_CH4	TMR1_CH3N	19
PB2 (PB2,BOOT1)	I/O	5T	-	-	20
PB10	I/O	5T	I2C2_SCL/ I2C4_SCL/ USART3_TX	TMR2_CH3	21
PB11	I/O	5T	I2C2_SDA/ I2C4_SDA/ USART3_RX	TMR2_CH4	22
V_{SS_1}	P	-	-	-	23
V_{DD_1}	P	-	-	-	24
PB12	I/O	5T	SPI2_NSS/ I2C2_SMBAI/ USART3_CK/ TMR1_BKIN(6)	-	25
PB13	I/O	5T	SPI2_SCK/ USART3_CTS/ TMR1_CH1N/	-	26
PB14	I/O	5T	SPI2_MISO/ USART3_RTS/ TMR1_CH2N/	-	27
PB15	I/O	5T	SPI2_MOSI/ TMR1_CH3N/	-	28
PA8	I/O	5T	USART1_CK/ TMR1_CH1/ MCO	-	29
PA9	I/O	5T	USART1_TX/ TMR1_CH2	-	30
PA10	I/O	5T	USART1_RX/ TMR1_CH3	-	31
PA11	I/O	5T	USART1_CTS/ USBD1DM/ USBD2DM/ CAN_RX/ TMR1_CH4	-	32

Name (Function after reset)	Type	Structure	Default multiplexing function	Remap	LQFP48
PA12	I/O	5T	USART1_RTS/ USBD1DP USBD2DP/ CAN_TX/ TMR1_ETR	-	33
PA13 (JTMS,SWDIO)	I/O	5T	-	PA13	34
V_{SS_2}	P		-	-	35
V_{DD_2}	P		-	-	36
PA14 (JTCK,SWCLK)	I/O	5T	-	PA14	37
PA15 (JTDI)	I/O	5T	-	TMR2_CH1_ETR/ PA15/ SPI1_NSS	38
PB3 (JTDO)	I/O	5T	-	PB3/ TRACESWO/ TMR2_CH2/ SPI1_SCK	39
PB4 (NJTRST)	I/O	5T	-	PB4/ TMR3_CH1/ SPI1_MISO	40
PB5	I/O	STD	I2C1_SMBAI	TMR3_CH2/ SPI1_MOSI	41
PB6	I/O	5T	I2C1_SCL/ I2C3_SCL/ TMR4_CH1	USART1_TX	42
PB7	I/O	5T	I2C1_SDA/ I2C3_SDA/ TMR4_CH2	USART1_RX	43
BOOT0	I	B	-	-	44
PB8	I/O	5T	TMR4_CH3	I2C1_SCL/ （I2C3_SCL） /CAN_RX	45
PB9	I/O	5T	TMR4_CH4	I2C1_SDA （I2C3_SDA） /CAN_TX	46
V_{SS_3}	P	-	-	-	47
V_{DD_3}	P	-	-	-	48

Note:

(1) PC13, PC14 and PC15 are powered through the power switch. Since the switch only sinks limited current (3mA), the use of GPIO from PC13 to PC15 in output mode is limited:

① The speed shall not exceed 2MHz when the heavy load is 30pF;

② Not used for current source (e.g. driving LED).

(2) For Pin 5 and Pin 6 of LQFP48 package, the default configuration after the chip is reset is OSC_IN and OSC_OUT, the software can reset these two pins with PD0 and PD1 functions;

4. Functional description

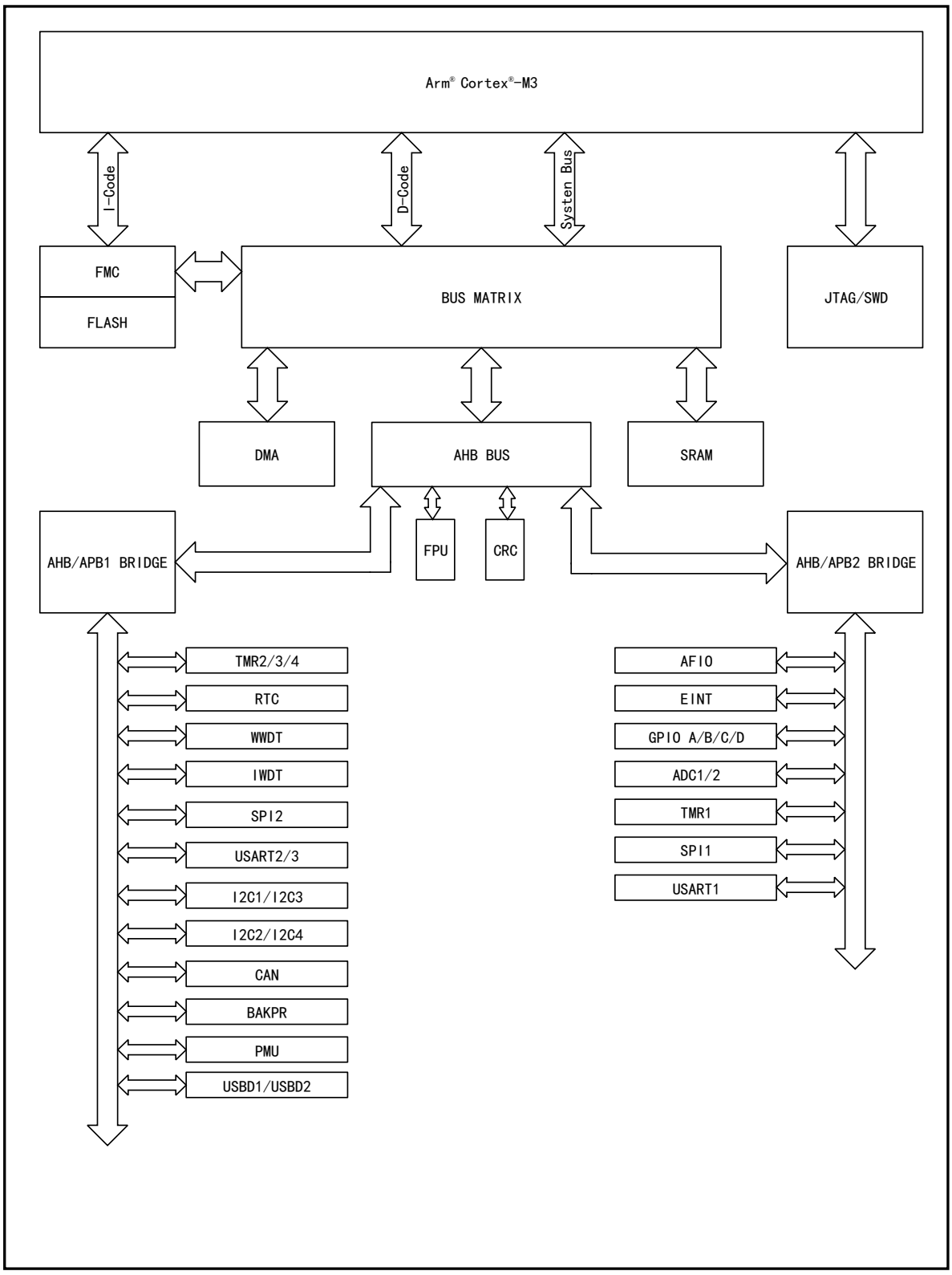
This chapter mainly introduces the system architecture, interrupt, on-chip memory, clock, power supply and peripheral features of APM32A103CBT7 series products; for information about the Arm® Cortex®-M3 core, please refer to the Arm® Cortex®-M3 technical reference manual, which can be downloaded from Arm's website.

Currently, the APM32A103CBT7 model has passed the AEC-Q100-Rev-H Grade2 standard.

4.1. System architecture

4.1.1. System block diagram

Figure 2 APM32A103CBT7 System Block Diagram



4.1.2. Address mapping

Table 4 APM32A103CBT7 Series Address Mapping Diagram

Region	Start Address	Peripheral Name
Code	0x0000 0000	Mapping area
Code	0x0800 0000	Flash
Code	0x0802 0000	Reserved
Code	0x1FFF F000	System Memory
Code	0x1FFF F800	Option Bytes
Code	0x1FFF F810	Reserved
SRAM	0x2000 0000	SRAM
APB1 bus	0x4000 0000	TMR2
APB1 bus	0x4000 0400	TMR3
APB1 bus	0x4000 0800	TMR4
APB1 bus	0x4000 0C00	Reserved
APB1 bus	0x4000 2800	RTC
APB1 bus	0x4000 2C00	WWDT
APB1 bus	0x4000 3000	IWDT
APB1 bus	0x4000 3400	Reserved
APB1 bus	0x4000 3800	SPI2
APB1 bus	0x4000 3C00	Reserved
APB1 bus	0x4000 4400	USART2
APB1 bus	0x4000 4800	USART3
APB1 bus	0x4000 4C00	Reserved
APB1 bus	0x4000 5400	I2C1(I2C3)
APB1 bus	0x4000 5800	I2C2(I2C4)
APB1 bus	0x4000 5C00	USBD1(USBD2)
APB1 bus	0x4000 6000	USBD/CAN SRAM
APB1 bus	0x4000 6400	CAN
APB1 bus	0x4000 6800	Reserved
APB1 bus	0x4000 6C00	BAKPR
APB1 bus	0x4000 7000	PMU
—	0x4000 7400	Reserved
APB2 bus	0x4001 0000	AFIO
APB2 bus	0x4001 0400	EINT
APB2 bus	0x4001 0800	Port A
APB2 bus	0x4001 0C00	Port B
APB2 bus	0x4001 1000	Port C
APB2 bus	0x4001 1400	Port D
APB2 bus	0x4001 1800	Reserved

Region	Start Address	Peripheral Name
APB2 bus	0x4001 2400	ADC1
APB2 bus	0x4001 2800	ADC2
APB2 bus	0x4001 2C00	TMR1
APB2 bus	0x4001 3000	SPI1
APB2 bus	0x4001 3400	Reserved
APB2 bus	0x4001 3800	USART1
APB2 bus	0x4001 3C00	Reserved
AHB bus	0x4002 0000	DMA
AHB bus	0x4002 0400	Reserved
AHB bus	0x4002 1000	RCM
AHB bus	0x4002 1400	Reserved
AHB bus	0x4002 2000	Flash Interface
AHB bus	0x4002 2400	Reserved
AHB bus	0x4002 3000	CRC
AHB bus	0x4002 3400	Reserved
AHB bus	0x4002 4000	FPU
AHB bus	0x4002 4400	Reserved
AHB bus	0xA000 0000	Reserved
—	0xA000 2000	Reserved

4.1.3. Startup configuration

At startup, the user can select one of the following three startup modes by setting the high and low levels of the Boot pin:

- Startup from main memory
- Startup from BootLoader
- Startup from built-in SRAM

The user can use USART interface to reprogram the user Flash if boot from BootLoader.

4.2. Core

The core of APM32A103CBT7 is Arm® Cortex®-M3. Based on this platform, the development cost is low and the power consumption is low. It can provide excellent computing performance and advanced system interrupt response, and is compatible with all Arm tools and software.

4.3. Interrupt controller

4.3.1. Nested Vector Interrupt Controller (NVIC)

It embeds a nested vectored interrupt controller (NVIC) that can handle up to 47 maskable interrupt channels (not including 16 interrupt lines of Cortex®-M3) and 16 priority levels. The interrupt vector entry address can be directly transmitted to the core, so that the interrupt response processing with low delay can give priority to the late higher priority interrupt.

4.3.2. External Interrupt/Event Controller (EINT)

The external interrupt/event controller consists of 19 edge detectors, and each detector includes edge detection circuit and interrupt/event request generation circuit; each detector can be configured as rising edge trigger, falling edge trigger or both and can be masked independently. Up to 37 GPIOs can be connected to the 16 external interrupt lines.

4.4. On-chip memory

On-chip memory includes main memory area, SRAM and information block; the information block includes system memory area and option byte; the system memory area stores BootLoader, 96-bit unique device ID and capacity information of main memory area; the system memory area has been written into the program and cannot be erased.

Table 5 On-chip Memory Area

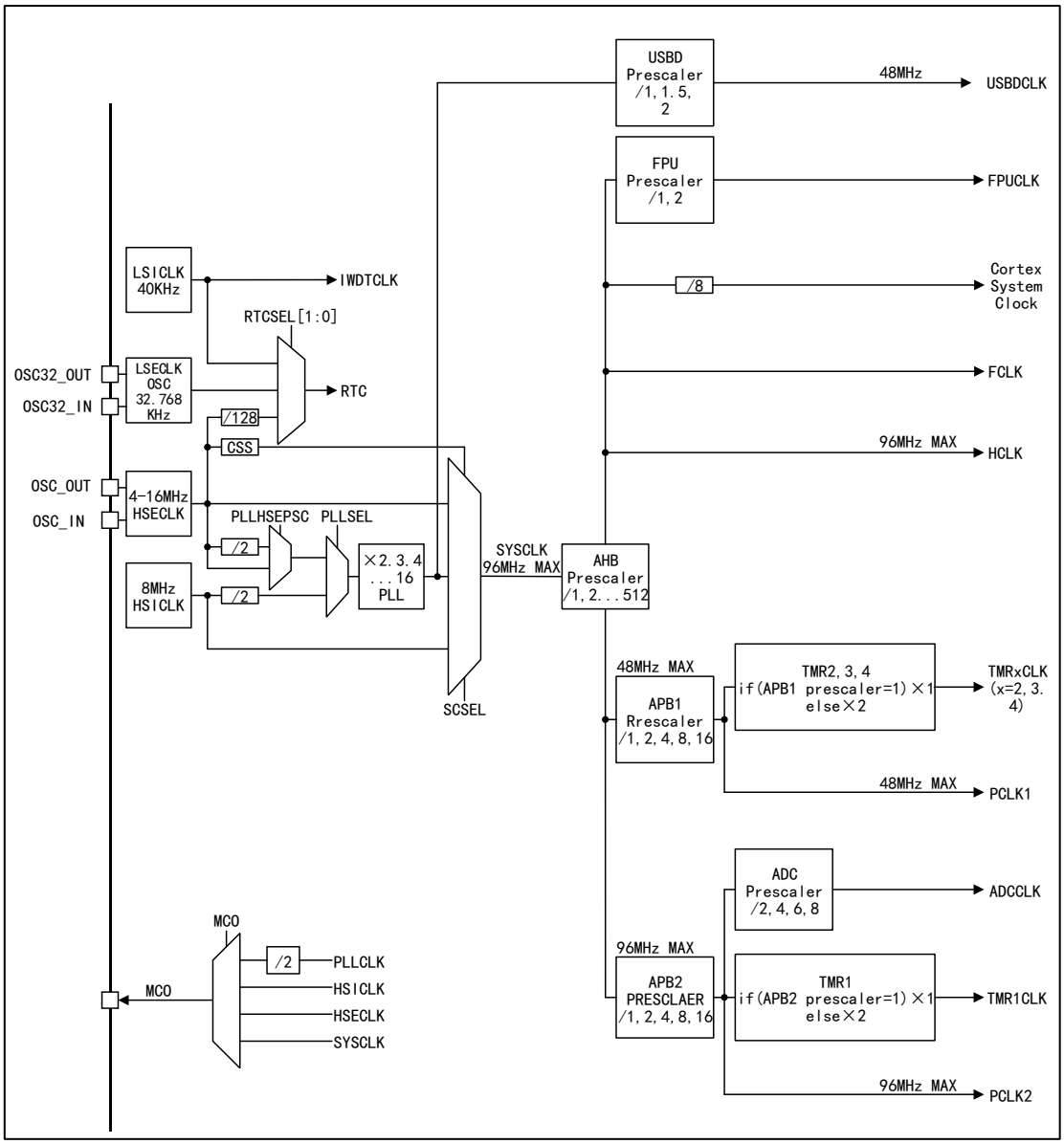
Memory	Maximum capacity	Function
Main memory area	128 KB	Store user programs and data.
SRAM	20 KB	CPU can access at 0 waiting cycle (read/write).
System memory area	2KB	Store BootLoader, 96-bit unique device ID, and main memory area capacity information
Option byte	16Bytes	Configure main memory area read-write protection and MCU working mode

4.5. Clock

4.5.1. Clock tree

Clock tree of APM32A103CBT7 is shown in the figure below:

Figure 3 APM32A103CBT7 Clock Tree



4.5.2. Clock source

Clock source is divided into high-speed clock and low-speed clock according to the speed; the high-speed clock includes HSICLK and HSECLK, and the low-speed clock includes LSECLK and LSICLK; clock source is divided into internal clock and external clock according to the chip inside/outside; the internal clock includes HSICLK and LSICLK, and the external clock includes HSECLK and LSECLK, among which HSICLK is calibrated by the factory to ±1% accuracy.

4.5.3. System clock

HSICLK, PLLCLK and HSECLK can be selected as system clock; the clock source of PLLCLK can be one of HSICLK, and HSECLK; the required system clock can be obtained by configuring PLL clock multiplier factor and frequency dividing coefficient.

When the product is reset and started, HSICLK is selected as the system clock by default, and then the user can choose one of the above clock sources as the system clock by himself. When HSECLK failure is detected, the system will automatically switch to the HSICLK, and if an interrupt is enabled, the software can receive the related interrupt.

4.5.4. Bus clock

AHB, APB1 and ABP2 are built in. The clock source of AHB is SYSCLK, and the clock source of APB1 and APB2 is HCLK; the required clock can be obtained by configuring the frequency dividing coefficient. The maximum frequency of AHB and high-speed APB2 is 96MHz, and the maximum frequency of APB1 is 48MHz.

4.6. Power Supply and power management

4.6.1. Power supply scheme

Table 6 Power Supply Scheme

Name	Voltage range	Instruction
V_{DD}	2.0～3.6V	I/Os (see pin distribution diagram for specific IO) and internal voltage regulator are powered through V_{DD} pin.
V_{DDA}/V_{SSA}	2.0～3.6V	Power supply of ADC, DAC, reset module, RC oscillator and PLL analog part; when ADC or DAC is used, V_{DDA} shall not be less than 2.4V; V_{DDA} and V_{SSA} must be connected to V_{DD} and V_{SS}.
V_{BAT}	1.8～3.6V	When V_{DD} is closed, RTC, external 32KHz oscillator and backup register are supplied through internal power switch.

4.6.2. Voltage regulator

Table 7 Regulator Operating Mode

Name	Instruction
Master mode (MR)	Used in run mode
Low-power mode (LPR)	Used in stop mode
Power-down mode	Used in standby mode, when the voltage regulator has high impedance output, the core circuit is powered down, the power consumption of the voltage regulator is zero, and all data of registers and SRAM will be lost.

Note: The voltage regulator is always in working state after reset, and outputs with high impedance in power-down mode.

4.6.3. Power supply voltage monitor

Power-on reset (POR) and power-down reset (PDR) circuits are integrated inside the product. These two circuits are always in working condition. When the power-down reset circuit monitors that the power supply voltage is lower than the specified threshold value ($V_{POR/PDR}$), even if the external reset circuit is used, the system will remain reset.

The product has a built-in programmable voltage regulator (PVD) that can monitor V_{DD} and compare it with V_{PVD} threshold. When V_{DD} is outside the V_{PVD} threshold range and the interrupt is enabled, the MCU can be set to a safe state through the interrupt service program.

4.7. Low-power mode

APM32A103CBT7 supports three low-power modes, namely, sleep mode, stop mode and standby mode, and there are differences in power, wake-up time and wake-up mode among these three modes. The low-power mode can be selected according to the actual application requirements.

Table 8 Low Power Consumption Mode

Mode	Instruction
Sleep mode	The core stops working, all peripherals are working, and it can be woken up through interrupts/events

Mode	Instruction
Stop mode	Under the condition that SRAM and register data are not lost, the stop mode can achieve the lowest power consumption; The clock of the internal 1.6V power supply module will stop, HSECLK crystal resonator, HSICLK and PLL will be prohibited, and the voltage regulator can be configured in normal mode or low power mode; Any external interrupt line can wake up MCU, and the external interrupt lines include one of the 16 external interrupt lines, PVD output, RTC and USBD.
Standby mode	The power consumption in this mode is the lowest; Internal voltage regulator is turned off, all 1.6V power supply modules are powered off, HSECLK crystal resonator, HSICLK and PLL clocks are turned off, SRAM and register data disappear, RTC area and backup register contents remain, and standby circuit still works; The external reset signal on NRST, IWDT reset, rising edge on WKUP pin or RTC event will wake MCU out of standby mode.

4.8. Floating Point Unit (FPU)

The product has an embedded independent FPU floating-point arithmetic processing unit that supports the IEEE754 standard and supports single-precision floating-point operations.

4.9. DMA

1 built-in DMA; DMA supports 7 channels. Each channel supports multiple DMA requests, but only one DMA request is allowed to enter the DMA channel at the same time. The peripherals supporting DMA requests are ADC, SPI, USART, I2C, and TMRx. Four levels of DMA channel priority can be configured. Support "memory→memory, memory→peripheral, peripheral→memory" transfer of data (the memory includes Flash、SRAM)

4.10. GPIO

GPIO can be configured as general input, general output, multiplexing function and analog input、output. The general input can be configured as floating input, pull-up input and pull-down input; the general output can be configured as push-pull output and open-drain output; the multiplexing function can be used for digital peripherals; and the analog input and output can be used for analog peripherals and low-power mode; the enable and disable pull-up/pull-down resistor can be configured; the speed of 2MHz, 10MHz and 50MHz can be configured; the higher the speed is, the greater the power and the noise will be.

4.11. Communication peripherals

4.11.1. USART

Up to 3 USART in the chip. The USART1 interface can communicate at a rate of 4.5Mbit/s, while other USART interfaces can communicate at a rate of 2.25Mbit/s. All USART interfaces can configure baud rate, parity check bit, stop bit, and data bit length; all the other USART can support DMA.

4.11.2. I2C

I2C1/2 both can work in multiple master modes or slave modes, support 7-bit or 10-bit addressing, and support dual-slave addressing in 7-bit slave mode; the communication rate supports standard mode (up to 100kbit/s) and fast mode (up to 400kbit/s); hardware CRC generator/checker are built in; they can operate with DMA and support SMBus 2.0 version/PMBus.

I2C3/4 bus is a two-wire serial interface, which is composed of serial data line (SDA) and serial clock (SCL). It can work as "transmitter" and "receiver", and can operate in standard mode, fast mode, fast mode and high-speed mode; In addition, high-speed mode and fast mode devices

are backward compatible.

4.11.3. SPI

Two built-in SPIs, support full duplex and half duplex communication in master mode and slave mode, can use DMA controller, and can configure 4~16 bits per frame, and communicate at a rate of up to 18Mbit/s.

4.11.4. CAN

1 built-in CAN, compatible with 2.0A and 2.0B (active) specification, and can communicate at a rate of up to 1Mbit/s. It can receive and send standard frame of 11-bit identifier and extended frame of 29-bit identifier. It has 3 sending mailboxes and 2 receiving FIFO, 14 3-level adjustable filters.

4.11.5. USBD

The product embeds USBD modules (USBD1 and USBD2) compatible with full-speed USBD devices, which comply with the standard of full-speed USBD devices (12Mb/s), and the endpoints can be configured by software, and have standby/wake-up functions. The dedicated 48MHz clock for USBD is directly generated by internal PLL. When using the USBD function, the system clock can only be one of 48MHz, 72MHz and 96MHz , which can obtain 48MHz required for USBD through 1 fractional frequency, 1.5 fractional frequency and 2 fractional frequency respectively.

USBD1 and USBD2 share register address and pin interface, so only one of them can be used at the same time.

4.11.6. Simultaneous Use of USBD Interface and CAN Interface:

When USBD and CAN are used together, you need to:

- Write 0x00000001 at the base address offset 0x100 of the USBD.
- The PA11 and PA12 pins are for USBD and CAN is used to multiplex other pins.

4.12. Analog peripherals

4.12.1. ADC

2 built-in ADCs with 12-bit accuracy, up to 10 external channels and 1 internal channel for each ADC. The internal channel measures the reference voltage respectively. A/D conversion mode of each channel has single, continuous, scan or intermittent modes, ADC conversion results can be left aligned or right aligned and stored in 16-bit data register; they support analog watchdog, and DMA.

4.12.1.1. Internal reference voltage

Built-in reference voltage V_{REFINT}, internally connected to ADC_IN17 channel, which can be obtained through ADC; V_{REFINT} provides stable voltage output for ADC.

4.13. Timer

1 built-in 16-bit advanced timers (TMR1), 3 general-purpose timers (TMR2/3/4), 1 independent watchdog timer, 1 window watchdog timer and 1 system tick timer.

Watchdog timer can be used to detect whether the program is running normally.

The system tick timer is the peripheral of the core with automatic reloading function. When the counter is 0, it can generate a maskable system interrupt, which can be used for real-time operating system and general delay.

Table 9 Function Comparison between Advanced/General-purpose/Basic and System Tick Timers

Timer type	System tick timer	General-purpose timer			Advanced timer
Timer name	Sys Tick Timer	TMR2	TMR3	TMR4	TMR1
Counter resolution	24-bit	16-bit			16-bit
Counter type	Down	Up, down, up/down			Up, down, up/down
Prescaler coefficient	-	Any integer between 1 and 65536			Any integer between 1 and 65536
General DMA request	-	OK			OK
Capture/Comparison channel	-	4			4
Complementary outputs	-	No			Yes
Pin characteristics	-	There are 5 pins in total: 1-way external trigger signal input pins, 4-way channel (non-complementary channel) pins			There are 9 pins in total: 1-way external trigger signal input pins, 1-way braking input signal pins, 3-pair complementary channel pins, 1-way channel (non-complementary channel) pins
Function Instruction	Special for real-time operating system Automatic reloading function supported When the counter is 0, it can generate a maskable system interrupt Can program the clock source	Synchronization or event chaining function provided Timers in debug mode can be frozen. Can be used to generate PWM output Each timer has independent DMA request generation. It can handle incremental encoder signals			It has complementary PWM output with dead band insertion When configured as a 16-bit standard timer, it has the same function as the TMRx timer. When configured as a 16-bit PWM generator, it has full modulation capability (0~100%). In debug mode, the timer can be frozen, and PWM output is disabled. Synchronization or event chaining function provided.

Table 10 Independent Watchdog and Window Watchdog Timers

Name	Counter resolution	Counter type	Prescaler coefficient	Functional Description
Independent watchdog	12-bit	Down	Any integer between 1 and 256	The clock is provided by an internally independent RC oscillator of 40KHz, which is independent of the master clock, so it can run in stop and standby modes. The whole system can be reset in case of problems.

Name	Counter resolution	Counter type	Prescaler coefficient	Functional Description
				It can provide timeout management for applications as a free-running timer. It can be configured as a software or hardware startup watchdog through option bytes. Timers in debug mode can be frozen.
Window watchdog	7-bit	Down	-	Can be set for free running. The whole system can be reset in case of problems. Driven by the master clock, it has early interrupt warning function; Timers in debug mode can be frozen.

4.14. RTC

1 RTC is built in, and there are LSECLK signal input pins (OSC32_IN and OSC32_OUT) and 1 TAMP input signal detection pin (TAMP); the clock source can select external 32.768kHz crystal oscillator, resonator or oscillator, LSICLK and HSECLK/128; it is supplied by V_{DD} by default; when V_{DD} is powered off, it can be automatically switched to V_{BAT} power supply, and RTC configuration and time data will not be lost; RTC configuration and time data are not lost in case of system resetting, software resetting and power resetting; it supports clock and calendar functions.

4.14.1. Backup register

84Bytes backup register is built in, and is supplied by V_{DD} by default; when V_{DD} is powered off, it can be automatically switched to V_{BAT} power supply, and the data in backup register will not be lost; the data in backup register will not be lost in case of system resetting, software resetting and power resetting.

4.15. CRC

A CRC (cyclic redundancy check) calculation unit is built in, which can generate CRC codes and operate 8-bit, 16-bit and 32-bit data.

5. Electrical characteristics

5.1. Test conditions of electrical characteristics

5.1.1. Maximum and minimum values

Unless otherwise specified, all products are tested on the production line at T_A=25℃. Its maximum and minimum values can support the worst environmental temperature, power supply voltage and clock frequency.

In the notes at the bottom of each table, it is stated that the data are obtained through comprehensive evaluation, design simulation or process characteristics and are not tested on the production line; on the basis of comprehensive evaluation, after passing the sample test, take the average value and add and subtract three times the standard deviation (average ±3∑) to get the maximum and minimum values.

5.1.2. Typical values

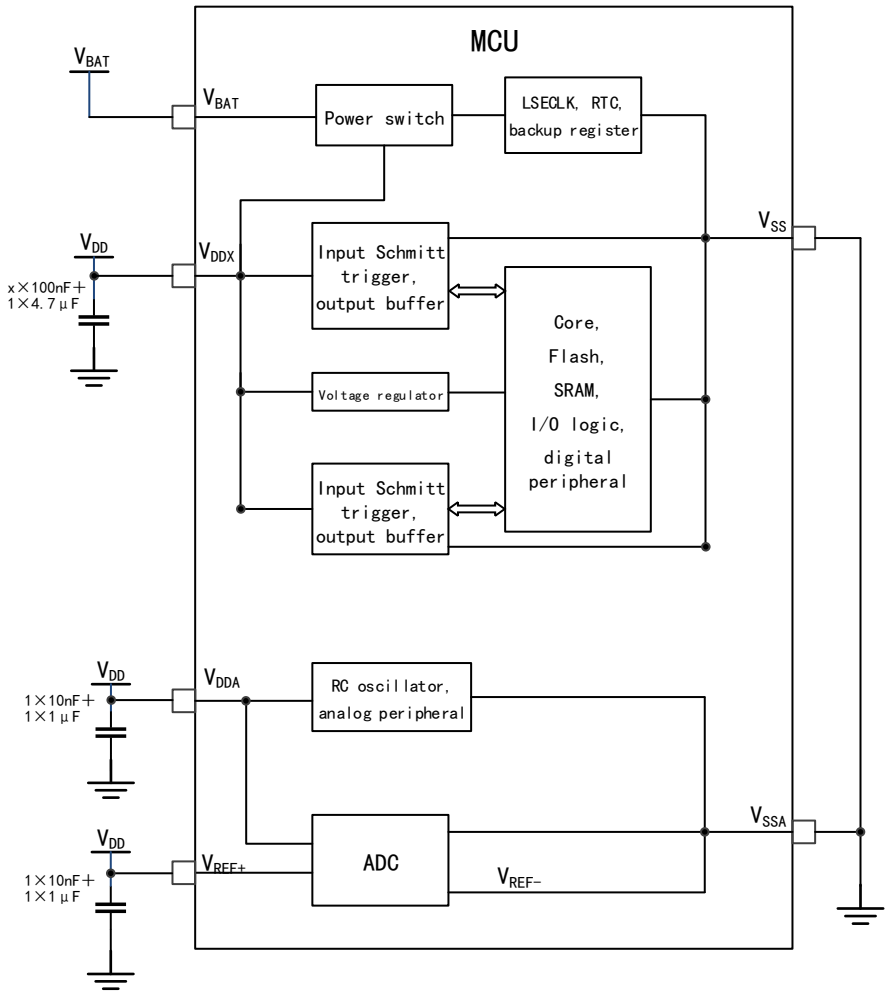
Unless otherwise specified, typical data are measured based on TA=25℃, V_{DD}=V_{DDA}=3.3V. these data are only used for design guidance.

5.1.3. Typical curve

Unless otherwise specified, typical curves will only be used for design guidance and will not be tested.

5.1.4. Power supply scheme

Figure 4 Power Supply Scheme



Notes: $V_{DD}x$ in the figure means the number of V_{DD} is x

5.1.5. Load capacitance

Figure 5 Load conditions when measuring pin parameters

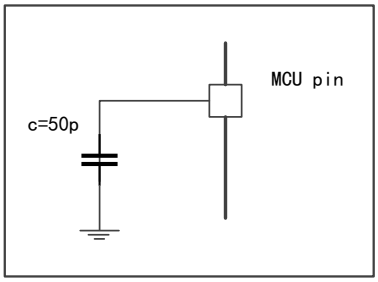


Figure 6 Pin Input Voltage Measurement Scheme

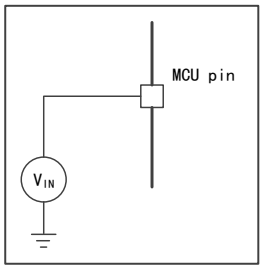
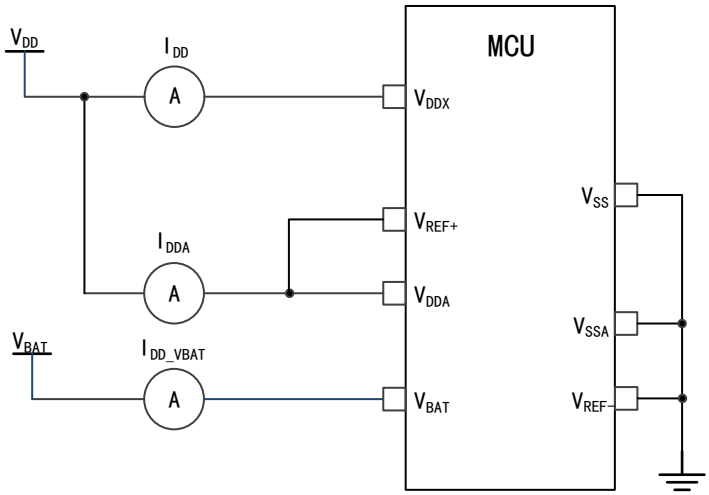


Figure 7 Power Consumption Measurement Scheme



5.2. Test under general operating conditions

Table 11 General Operating Conditions

Symbol	Parameter	Conditions	Minimum value	Maximum value	Unit
f_{HCLK}	Internal AHB clock frequency	-	-	96	MHz
f_{PCLK1}	Internal APB1 clock frequency	-	-	48	
f_{PCLK2}	Internal APB2 clock frequency	-	-	96	
V_{DD}	Main power supply voltage	-	2	3.6	V
V_{DDA}	Analog power supply voltage (When neither ADC nor DAC is used)	Must be the same as V_{DD}	V_{DD}	3.6	V
	Analog power supply voltage (When ADC and DAC are used)		2.4	3.6	
V_{BAT}	Power supply voltage of backup domain	-	1.8	3.6	V
T_A	Ambient temperature (temperature number 7)	Maximum power dissipation	-40	105	℃

5.3. Absolute maximum ratings

If the load on the device exceeds the absolute maximum rating, it may cause permanent damage to the device. Here, only the maximum load that can be borne is given, and there is no guarantee that the device functions normally under this condition.

5.3.1. Maximum temperature characteristics

Table 12 Temperature Characteristics

Symbol	Description	Numerical Value	Unit
T_{STG}	Storage temperature range	-55 ~ +150	℃
T_J	Maximum junction temperature	150	℃

5.3.2. Maximum rated voltage characteristics

All power supply (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the power supply within the external limited range.

Table 13 Maximum Rated Voltage Characteristics

Symbol	Description	Minimum value	Maximum value	Unit
V_{DD} - V_{SS}	External main power supply voltage	-0.3	4.0	V
V_{DDA}-V_{SSA}	External analog power supply voltage	-0.3	4.0	
V_{BAT}-V_{SS}	Power supply voltage of external backup domain	-0.3	4.0	
V_{DD}-V_{DDA}	Voltage difference allowed by V_{DD}>V_{DDA}	-	0.3	
V_{IN}	Input voltage on FT pins	V_{SS}-0.3	5.5	
	Input voltage on other pins	V_{SS}-0.3	V_{DD} + 0.3	
| ΔV_{DDx} |	Voltage difference between different power supply pins	-	50	mV
| V_{SSx}-V_{SS} |	Voltage difference between different grounding pins	-	50	

5.3.3. Maximum rated current features

Table 14 Current Characteristics

Symbol	Description	Maximum	Unit
I_{VDD}	Total current (supply current) (1) went through the V_{DD}/V_{DDA} power cord.	150	mA
I_{VSS}	Total current (outflow current) (1) went through the V_{SS} ground cord.	150	
I_{IO}	Irrigation current on any I/O and control pins	25	
	Pull current on any I/O and control pins	-25	
$I_{INJ(PIN)}$ (2) (3)	Injection current of NRST pin	±5	
	Injection current of HSECLK's OSC_IN pin and LSECLK's OSC_IN pin	±5	
	Injection current of other pins(4)	±5	
$\Sigma I_{INJ(PIN)}$(2)	Total injection current on all I/O and control pins(5)	±25	

Note:

(1) All power supplies (V_{DD}, V_{DDA}) and grounds (V_{SS}, V_{SSA}) must always be within the allowable range.

(2) The outflow current will interfere with the analog performance of the device

(3) I/O cannot be positive injected; When V_{IN}<V_{SS}, $I_{INJ\ (PIN)}$ cannot exceed the maximum allowable input voltage

(4) If the V_{IN} exceeds the maximum value, the $I_{INJ\ (PIN)}$ must be externally restricted from exceeding its maximum value. When V_{IN}>V_{DD}, the current flows into the pin; When V_{IN}<V_{SS}, the current flows out of the pin.

(5) When several I/O ports have injected current at the same time, The maximum value of ΣIINJ (PIN) is the sum of the instantaneous absolute values of the inflow current and the outflow current.

5.3.4. Electrostatic discharge (ESD)

Table 15 ESD Absolute Maximum Ratings

Symbol	Parameter	Conditions	Maximum value	Unit
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charging device model)	T_A = +18~24 ℃，conforming to AEC-Q100-011	750	V

Note: The samples are measured by a third-party testing organization and are not tested in production.

5.3.5. Static latch-up (LU)

Table 16 Static Latch-up

Symbol	Parameter	Conditions	Type
LU	Class of static latch-up	T_A = +105℃, conforming to AEC-Q100-004	CLASS Ⅱ A

Note: The samples are measured by a third-party testing organization and are not tested in production.

5.4. On-chip memory

5.4.1. Flash characteristics

Table 17 Flash Memory Characteristics

Symbol	Parameter	Conditions	Minimum value	Typical values	Maximum value	Unit
t_{prog}	16-bit programming time	T_A = -40~105℃ V_{DD}=2.4~3.6V	15	20.46	40	μs
t_{ERASE}	Page (2KBytes) erase time	T_A = -40~105℃ V_{DD}=2.4~3.6V	1	-	10	ms
t_{ME}	Whole erase time	T_A = -40~105℃ V_{DD}=2.4~3.6V	5	-	20	ms
V_{prog}	Programming voltage	T_A = -40~105℃	2	-	3.6	V

Note: It is obtained from a comprehensive evaluation and is not tested in production.

5.5. Clock

5.5.1. Characteristics of external clock source

5.5.1.1.1. High-speed external clock generated by crystal resonator

For detailed parameters (frequency, package, precision, etc.) of crystal resonator, please consult the corresponding manufacturer.

Table 18 HSECLK4~16MHz Oscillator Characteristics

Symbol	Parameter	Conditions	Minimum value	Typical values	Maximum value	Unit
f_{OSC_IN}	Oscillator frequency	-	4	8	16	MHz
R_F	Feedback resistance	-	-	310	-	kΩ

Symbol	Parameter	Conditions	Minimum value	Typical values	Maximum value	Unit
$I_{DD(HSECLK)}$	HSECLK current consumption	V_{DD}=3.3V, C_L=10pF@8MHz	-	374	-	μA
I_2	Drive current	-	-	-	1.25	mA
$t_{SU(HSECLK)}$	Startup time	V_{DD} is stable	-	1	-	ms
$Duty_{(HSECLK)}$	HSECLK duty cycle	-	45	-	60	%

Note: It is obtained from a comprehensive evaluation and is not tested in production.

5.5.1.1.2. Low-speed external clock generated by crystal resonator

For detailed parameters (frequency, package, precision, etc.) of crystal resonator, please consult the corresponding manufacturer.

Table 19 LSECLK Oscillator Characteristics (f_{LSECLK}=32.768KHz)

Symbol	Parameter	Conditions	Minimum value	Typical values	Maximum value	Unit
f_{OSF_IN}	Oscillator frequency	-	-	32.768	-	KHz
$I_{DD(LSECLK)}$	LSECLK current consumption	-	-	0.74	-	μA
I_2	Drive current	-	-	-	0.37	μA
$t_{SU(LSECLK)}$(1)	Startup time	V_{DDIOx} is stable	-	2	-	s

Note: It is obtained from a comprehensive evaluation and is not tested in production.

（1） $t_{SU(LSECLK)}$ is the startup time, which is measured from the time when LSECLK is enabled by software to the time when stable oscillation at 32.768KHz is obtained. This value is measured using a standard crystal resonator, which may vary greatly due to different crystal manufacturers.

5.5.2. Characteristics of internal clock source

5.5.2.1.1. High speed internal (HSICLK) RC oscillator

Table 20 HSICLK Oscillator Characteristics

Symbol	Parameter	Conditions		Min	Type	Max	Unit
f_{HSICLK}	Frequency	-		-	8	-	MHz
Acc_{HSICLK}	Accuracy of HSICLK oscillator	Factory calibration	V_{DD}=3.3V，T_A=25℃(1)	-1	-	1	%
			V_{DD}=2-3.6V，T_A=-40~105℃	-1.5	-	2	%
$I_{DDA(HSICLK)}$	Power consumption of HSICLK oscillator	-		-	-	140	μA
$t_{SU(HSICLK)}$	Startup time of HSICLK oscillator	V_{DD}=3.3V，T_A=-40~105℃		1	-	2.4	μs

Note: It is obtained from a comprehensive evaluation and is not tested in production.

5.5.2.1.2. Low speed internal (LSICLK) RC oscillator

Table 21 LSICLK Oscillator Characteristics

Symbol	Parameter	Min	Type	Max	Unit
f_{LSICLK}	Frequency (V_{DD} =2-3.6V, T_A =-40~105℃)	30	42	60	KHz
$I_{DD(LSICLK)}$	Power consumption of LSICLK oscillator	-	0.66	-	μA
$t_{SU(LSICLK)}$	LSICLK oscillator startup time, (V_{DD}=3.3V, T_A=-40~105℃)	-	-	80	μs

Note: It is obtained from a comprehensive evaluation and is not tested in production.

5.5.3. PLL Characteristics

Table 22 PLL Characteristics

Symbol	Parameter	Numerical Value			Unit
		Minimum value	Typical values	Maximum value	
f_{PLL_IN}	PLL input clock	1	8	25	MHz
	PLL input clock duty cycle	40	-	60	%
f_{PLL_OUT}	PLL frequency doubling output clock, (V_{DD}=3.3V, T_A=-40~105℃)	16	-	96	MHz
t_{LOCK}	PLL phase locking time	-	-	200	μs

Note: It is obtained from a comprehensive evaluation and is not tested in production.

5.6. Reset and power management

5.6.1. Test of embedded reset and power control block characteristics

Table 23 Embedded Reset and Power Control Block Characteristics

Symbol	Parameter	Conditions	Minimum value	Typical values	Maximum value	Unit
$V_{POR/PDR}$	Power-on/power-down reset threshold	Falling edge	1.86	1.87	1.95	V
		Rising edge	1.92	1.93	2.01	V
$V_{PDRhyst}$	PDR hysteresis	-	50.00	60.00	70.00	mV
$T_{RSTTEMPO}$	Reset duration	-	0.90	-	2.4	ms

Note: It is obtained from a comprehensive evaluation and is not tested in production.

Table 24 Programmable Power Supply Voltage Detector Characteristics

Symbol	Parameter	Conditions	Minimum value	Typical values	Maximum value	Unit
V_{PVD}	Programmable power supply voltage detector	PLS[2:0]=000 (rising edge)	2.18	2.20	2.25	V
		PLS[2:0]=000 (falling edge)	2.07	2.10	2.15	V
		PLS[2:0]=000(PVD hysteresis)	90	101.33	110	mV

Symbol	Parameter	Conditions	Minimum value	Typical values	Maximum value	Unit
	voltage level selection	PLS[2:0]=001 (rising edgeg)	2.28	2.31	2.36	V
		PLS[2:0]=001 (falling edge)	2.17	2.20	2.24	V
		PLS[2:0]=001(PVD hysteresis)	100	111	120	mV
		PLS[2:0]=010 (rising edgeg)	2.38	2.41	2.46	V
		PLS[2:0]=010 (falling edge)	2.27	2.30	2.35	V
		PLS[2:0]=010(PVD hysteresis)	90	107	110	mV
		PLS[2:0]=011 (rising edgeg)	2.47	2.50	2.56	V
		PLS[2:0]=011 (falling edge)	2.37	2.40	2.45	V
		PLS[2:0]=011(PVD hysteresis)	80	102	110	mV
		PLS[2:0]=100 (rising edgeg)	2.57	2.61	2.66	V
		PLS[2:0]=100 (falling edge)	2.46	2.50	2.55	V
		PLS[2:0]=100(PVD hysteresis)	100	111	120	mV
		PLS[2:0]=101 (rising edgeg)	2.67	2.70	2.76	V
		PLS[2:0]=101 (falling edge)	2.56	2.60	2.66	V
		PLS[2:0]=101(PVD hysteresis)	90	103.33	110	mV
		PLS[2:0]=110 (rising edgeg)	2.77	2.81	2.87	V
		PLS[2:0]=110 (falling edge)	2.66	2.70	2.75	V
		PLS[2:0]=110(PVD hysteresis)	90	110.33	120	mV
		PLS[2:0]=111 (rising edgeg)	2.86	2.90	2.96	V
		PLS[2:0]=111 (falling edge)	2.76	2.80	2.86	V
		PLS[2:0]=111(PVD hysteresis)	80	100.67	110	mV

Note: It is obtained from a comprehensive evaluation and is not tested in production.

5.7. Power consumption

5.7.1. Power consumption test environment

（1） The values are measured by executing Dhrystone 2.1, with the Keil.V5 compilation environment and the L0 compilation optimization level.

（2） All I/O pins are in input mode with a static value at V_{DD} or V_{SS} (no load)

（3） Unless otherwise specified, all peripherals are turned off

（4） The relationship between Flash waiting cycle setting and f_{HCLK} :

0~24MHz: 0 waiting cycle

24~48MHz: 1 waiting cycle

48~72MHz: 2 waiting cycles

72~96MHz: 3 waiting cycles

（5） The instruction prefetch function is enabled (Note: it must be set before clock setting and bus frequency division)

（6） When the peripherals are enabled: $f_{PCLK1}=f_{HCLK}/2$，$f_{PCLK2}=f_{HCLK}$

5.7.2. Power consumption in run mode

Table 25 Power Consumption in Run Mode when the Program is Executed in Flash/RAM

Parameter	Conditions	f_{HCLK}	Typical value (1)		Maximum value (1)	
			T_A=25℃，V_{DD}=3.3V		T_A=105℃，V_{DD}=3.6V	
			I_{DDA}(μA)	I_{DD}(mA)	I_{DDA}(μA)	I_{DD}(mA)
Power consumption in run mode	HSECLK bypass (2), enabling all peripherals	96MHz	210.66	26.32	404.62	27.85
		72MHz	138.52	18.82	255.93	20.20
		48MHz	104.29	15.39	182.25	16.48
		36MHz	79.96	11.66	141.37	12.66
		24MHz	58.67	8.53	73.92	9.21
		16MHz	45.84	5.85	64.70	6.37
		8MHz	2.67	2.98	6.69	3.43
	HSECLK bypass (2), turning off all peripherals	96MHz	210.72	16.12	252.02	17.07
		72MHz	138.52	12.22	162.05	12.91
		48MHz	104.28	10.45	123.05	11.09
		36MHz	79.98	7.93	95.59	8.39
		24MHz	58.68	5.97	72.44	6.42
		16MHz	45.83	4.10	58.69	4.56
		8MHz	2.68	2.16	4.63	2.54
	HSICLK (2), enabling all peripherals	72MHz	138.11	17.27	159.29	18.53
		48MHz	104.02	13.09	122.51	14.06
		32MHz	79.79	9.91	93.89	10.47
		24MHz	58.52	6.78	71.35	7.33
		16MHz	45.69	4.64	57.85	5.06
		8MHz	2.66	2.39	4.42	2.65
	HSICLK (2), turning off all peripherals	72MHz	137.74	10.58	160.61	11.30
		48MHz	103.78	8.03	123.80	8.62
		32MHz	79.45	6.14	95.21	6.60
		24MHz	58.37	4.24	72.59	4.69
		16MHz	45.52	2.96	57.88	3.43
		8MHz	2.68	1.60	5.21	1.98

Note: (1) It is obtained from a comprehensive evaluation and is not tested in production.

(2) The external clock is 8MHz, and when f_{HCLK}>8MHz, turn on PLL, otherwise, turn off PLL.

5.7.3. Power consumption in sleep mode

Table 26 Power Consumption in Sleep Mode when the Program is Executed in Flash/RAM

Parameter	Conditions	f_{HCLK}	Typical value (1)		Maximum value (1)	
			T_A=25℃，V_{DD}=3.3V		T_A=105℃，V_{DD}=3.6V	
			I_{DDA}(μA)	I_{DD}(mA）	I_{DDA}(μA)	I_{DD}(mA)
Power consumption in sleep mode	HSECLK bypass (2) , enabling all peripherals	96 MHz	210.76	16.26	226.10	16.45
		72MHz	128.55	11.00	148.48	11.18
		48MHz	104.31	8.36	112.13	8.53
		36MHz	79.98	6.41	86.66	6.52
		24MHz	58.70	4.40	64.53	4.54
		16MHz	45.83	3.06	51.26	3.21
		8MHz	2.68	1.62	3.84	1.76
	HSECLK bypass (2) , turning off all peripherals	96 MHz	210.76	5.40	216.10	5.53
		72MHz	138.52	3.74	142.60	3.86
		48MHz	104.29	2.91	109.68	3.04
		36MHz	79.97	2.28	86.00	2.40
		24MHz	58.69	1.67	64.73	1.80
		16MHz	45.83	1.25	51.39	1.38
		8MHz	2.68	0.74	3.84	0.87

Note:

(1) It is obtained from a comprehensive evaluation and is not tested in production.

(2) The external clock is 8MHz, and when f_{HCLK}>8MHz, turn on PLL, otherwise, turn off PLL

5.7.4. Power consumption in stop mode and standby mode

Table 27 Power Consumption in Stop Mode and Standby Mode

Parameter	Conditions	Typical value (1), (T_A=25℃)						Maximum value (1), (V_{DD}=3.6V)		Unit
		V_{DD}=2.4V		V_{DD}=3.3V		V_{DD}=3.6V		T_A=105℃		
		I_{DDA}	I_{DD}	I_{DDA}	I_{DD}	I_{DDA}	I_{DD}	I_{DDA}	I_{DD}	
Power consumption in stop mode	Regulator in run mode, low-speed and high-speed internal RC oscillators and high-speed oscillator OFF(no independent watchdog)	2.15	22.164	2.672	22.369	2.86	23.198	5.486	178.636	μA
	Regulator in low-power mode, low-speed and high-speed internal RC oscillators and high-	2.149	9.688	2.672	9.884	2.867	10.006	4.524	155.871	

Parameter	Conditions	Typical value (1), (T_A=25℃)						Maximum value (1), (V_{DD}=3.6V)		Unit
		V_{DD}=2.4V		V_{DD}=3.3V		V_{DD}=3.6V		T_A=105℃		
		I_{DDA}	I_{DD}	I_{DDA}	I_{DD}	I_{DDA}	I_{DD}	I_{DDA}	I_{DD}	
	speed oscillator OFF(no independent watchdog)									
Power consumption in standby mode	Low-speed internal RC oscillator and independent watchdog ON	2.344	0.504	3.008	0.93	3.278	1.08	4.363	10.119	
	Low-speed internal RC oscillator on, independent watchdog OFF	2.342	0.383	3.009	0.757	3.277	0.911	4.31	9.854	
	Low-speed internal RC oscillator and independent watchdog OFF, low-speed oscillator and RTC OFF	1.996	0.163	2.519	0.355	2.716	0.475	3.94	9.511	

Note: (1) It is obtained from a comprehensive evaluation and is not tested in production.

5.7.5. Backup domain power consumption

Table 28 Backup Domain Power Consumption

Symbol	Conditions	Typical value (1), T_A=25℃			Maximum value (1), V_{BAT}=3.6V			Unit
		V_{BAT}=2.0V	V_{BAT}=2.4V	V_{BAT}=3.3V	T_A=25℃	T_A=85℃	T_A=105℃	
$I_{DD}\_V_{BAT}$	The low-speed oscillator and RTC are in ON state	1.106	1.268	1.704	1.956	2.568	3.256	μA

Note: (1) It is obtained from a comprehensive evaluation and is not tested in production.

5.7.6. Peripheral power consumption

The HSECLK Bypass 1M is adopted as clock source, f_{PCLK}=f_{HCLK}=1M.

Peripheral power consumption = current that enables the peripheral clock-current that disables the peripheral clock.

Table 29 Peripheral Power Consumption

Parameter	Peripheral	Typical value (1) T_A =25℃, V_{DD} =3.3V	Unit
AHB	DMA	0.53	mA
APB1	TMR2	0.67	
	TMR3	0.69	
	TMR4	0.62	
	WWDT	0.08	
	SPI2	0.07	

Parameter	Peripheral	Typical value (1) T_A =25℃, V_{DD} =3.3V	Unit
	USART2	0.27	
	USART3	0.27	
	I2C1	0.22	
	I2C2	0.22	
	USBD	0.48	
	CAN	0.37	
	BAKPR	0.06	
	PMU	0.06	
APB2	GPIOA	0.25	
	GPIOB	0.24	
	GPIOC	0.24	
	GPIOD	0.21	
	ADC1	0.63	
	ADC2	0.57	
	TMR1	0.96	
	SPI1	0.33	
	USART1	0.46	

Note: It is obtained from a comprehensive evaluation and is not tested in production.

5.8. Wake-up time in low power mode

The measurement of wake-up time in low power mode is from the start of wake-up event to the time when the user program reads the first instruction, in which V_{DD}=V_{DDA}.

Table 30 Wake Up Time in Low-power Mode

Symbol	Parameter	Conditions	Minimum value (T_A=25℃)	Typical value			Maximum value	Unit
				2V	3.3V	3.6V		
$t_{WUSLEEP}$	Wake-up from sleep mode	-	1.72	2.05	1.84	1.81	2.16	μs
t_{WUSTOP}	Wake up from stop mode	The voltage regulator is in run mode	3.46	3.92	3.57	3.52	4.00	
		The voltage regulator is in low power mode	4.60	6.50	4.92	4.74	7.00	
$t_{WUSTDBY}$	Wake up from standby mode	-	20.00	33.21	26.43	25.07	40.40	

Note: It is obtained from a comprehensive evaluation and is not tested in production.

5.9. Pin characteristics

5.9.1. I/O pin characteristics

Table 31 DC Characteristics (test condition of V_{DD}=2.7~3.6V, T_A=-40~105℃)

Symbol	Parameter	Conditions	Minimum value	Typical values	Maximum value	Unit
V_{IL}	Low level input voltage	CMOS port	-0.5	-	0.35V_{DD}	V
V_{IH}	High level input voltage		0.65V_{DD}	-	V_{DD}+0.5	
V_{IL}	Low level input voltage	TTL port	-0.5	-	0.8	
V_{IH}	Standard I/O pin, input high level voltage		2	-	V_{DD}+0.5	
	I/O FT pin, input high level voltage		2	-	5.5	
V_{hys}	Standard I/O Schmitt trigger voltage hysteresis	-	200	-	-	mV
	I/O FT Schmitt trigger voltage hysteresis		5%V_{DD}	-	-	mV
I_{lkg}	Input leakage current	$V_{SS} \le V_{IN} \le V_{DD}$ Standard I/O port	-	-	±1	μA
		V_{IN}=5V, I/O FT port	-	-	3	
R_{PU}	Weak pull-up equivalent resistance	V_{IN}=V_{SS}	30	40	50	kΩ
R_{PD}	Weak pull-down equivalent resistance	V_{IN}=V_{DD}	30	40	50	kΩ

Note: It is obtained from a comprehensive evaluation and is not tested in production.

Table 32 AC Characteristics

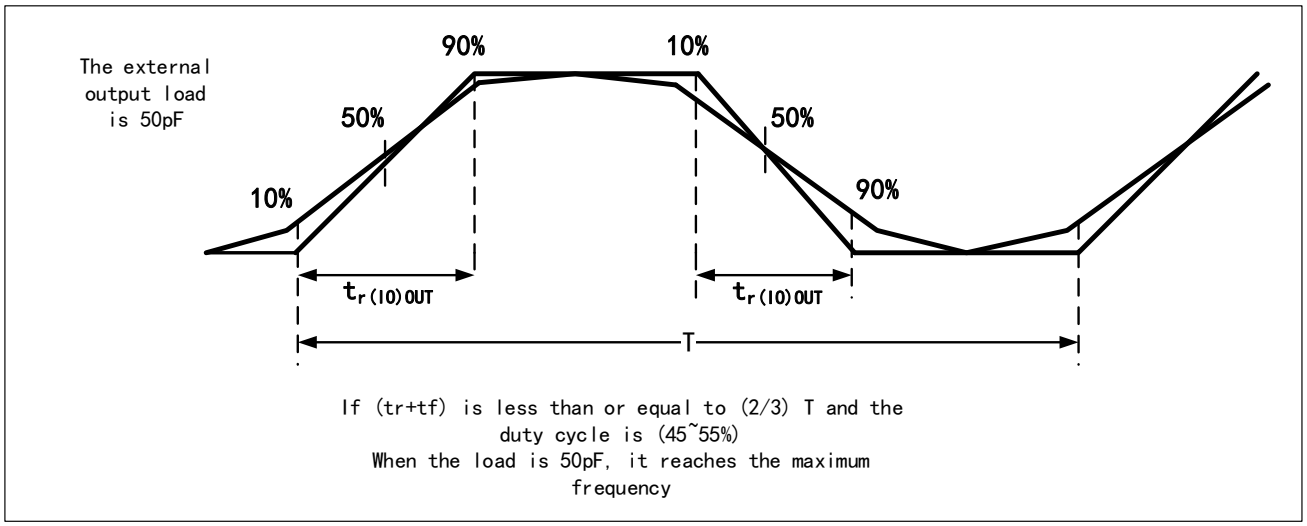
MODEy[1:0] Configuration	Symbol	Parameter	Conditions	Minimum value	Maximum value	Unit
10 (2MHz)	$f_{max(IO)out}$	Maximum frequency	CL=50 pF, V_{DD}=2~3.6V	-	2	MHz
	$t_{f(IO)out}$	Output fall time from high to low level	CL=50 pF, V_{DD} =2~3.6V	-	125	ns
	$t_{r(IO)out}$	Output rise time from low to high level		-	125	
01 (10MHz)	$f_{max(IO)out}$	Maximum frequency	CL=50 pF, V_{DD} =2~3.6V	-	10	MHz
	$t_{f(IO)out}$	Output fall time from high to low level	CL=50 pF, V_{DD} =2~3.6V	-	25	ns
	$t_{r(IO)out}$	Output rise time from low to high level		-	25	
11 (50MHz)	$f_{max(IO)out}$	Maximum frequency	CL=30 pF, V_{DD} =2.7~3.6V	-	50	MHz

MODEy[1:0] Configuration	Symbol	Parameter	Conditions	Minimum value	Maximum value	Unit
	$t_{f(IO)out}$	Output fall time from high to low level	CL=30 pF, V_{DD} =2.7~3.6V	-	5	ns
	$t_{r(IO)out}$	Output rise time from low to high level		-	5	

Note: (1) The rate of I/O port can be configured through MODEy.

(2) The data are obtained from a comprehensive evaluation and is not tested in production.

Figure 8 I/O AC Characteristics Definition



Note: According to the comprehensive evaluation, it is not tested in production.

Table 33 Output Drive Current Characteristics (test condition V_{DD}=2.7~3.6V, T_A=-40~105℃)

Symbol	Parameter	Conditions	Minimum value	Maximum value	Unit
V_{OL}	Output low level voltage for an I/O pin when 8 pins are sunk at same time	I_{IO} = +8mA 2.7V<V_{DD}<3.6V	-	0.49	V
V_{OH}	Output high level voltage for an I/O pin when 8 pins are sourced at same time		V_{DD}-0.4	-	
V_{OL}	Output low level voltage for an I/O pin when 8 pins are sunk at same time	I_{IO} = +20mA 2.7V<V_{DD}<3.6V	-	1.50	V
V_{OH}	Output high level voltage for an I/O pin when 8 pins are sourced at same time		V_{DD}-1.3	-	

5.9.2. NRST pin characteristics

The NRST pin input drive adopts CMOS process, which is connected with a permanent pull-up resistor R_{PU}.

Table 34 NRST Pin Characteristics (test condition V_{DD}=3.3V, T_A=-40~105℃)

Symbol	Parameter	Conditions	Min	Type	Max	Unit
$V_{IL(NRST)}$	NRST low level input voltage	-	-0.5	-	0.8	V
$V_{IH(NRST)}$	NRST high level input voltage	-	2	-	V_{DD}+0.5	

Symbol	Parameter	Conditions	Min	Type	Max	Unit
$V_{hys(NRST)}$	NRST Schmitt trigger voltage hysteresis	-	-	200	-	mV
RPU	Weak pull-up equivalent resistance	$V_{IN} = V_{SS}$	30	40	50	kΩ

Note: It is obtained from a comprehensive evaluation and is not tested in production.

5.10. Communication peripherals

5.10.1. I2C peripheral characteristics

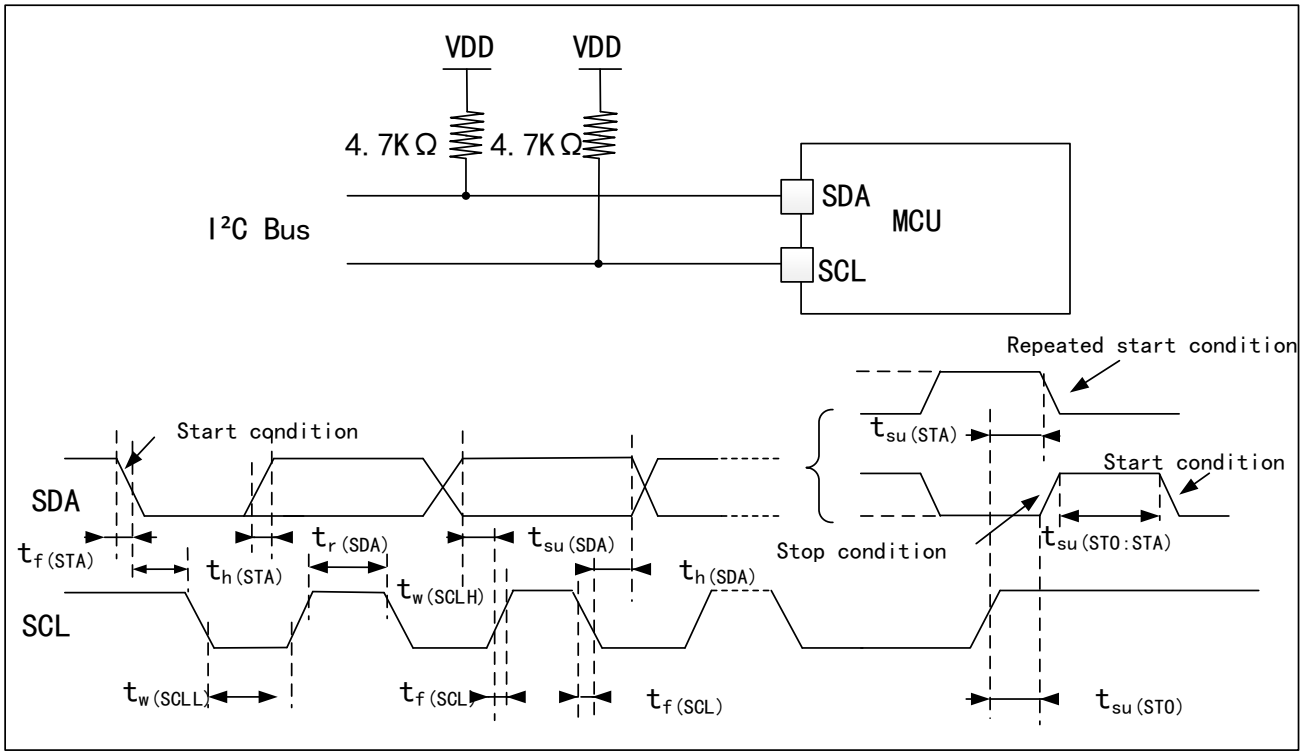
To achieve maximum frequency of I2C in standard mode, f_{PCLK1} must be greater than 2MHz. To achieve maximum frequency of I2C in fast mode, f_{PCLK1} must be greater than 4MHz.

Table 35 I2C Interface Characteristics (T_A=25℃, V_{DD}=3.3V)

Symbol	Parameter	Standard I2C		Fast I2C		Unit
		Min	Max	Min	Max	
$t_{w(SCLL)}$	SCL clock low time	4.7	-	1.3	-	μs
$t_{w(SCLH)}$	SCL clock high time	4.0	-	0.6	-	
$t_{su(SDA)}$	SDA setup time	250	-	100	-	ns
$t_{h(SDA)}$	SDA data hold time	-	503.65	-	900	
$t_{r(SDA)}/t_{r(SCL)}$	SDA and SCL rise time	-	1000	-	300	
$t_{f(SDA)}/t_{f(SCL)}$	SDA and SCL fall time	-	300	-	300	
$t_{h(STA)}$	Start condition hold time	4.0	-	0.6	-	μs
$t_{su(STA)}$	Repeated start condition setup time	4.7	-	0.6	-	
$t_{su(STO)}$	Setup time of stop condition	4.0	-	0.6	-	
$t_{w(STO:STA)}$	Time from stop condition to start condition (bus idle)	4.7	-	1.3	-	

Note: It is obtained from a comprehensive evaluation and is not tested in production.

Figure 9 I2C Bus AC Waveform and Measurement Circuit



Note: The measuring points are set at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

5.10.2. SPI peripheral characteristics

Table 36 SPI Characteristics (T_A=25℃, V_{DD}=3.3V)

Symbol	Parameter	Conditions	Minimum value	Maximum value	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	Master mode	-	18	MHz
		Slave mode	-	18	
$t_{r(SCK)}$ $t_{f(SCK)}$	SI clock rise and fall time	Load capacitance: C = 30pF	-	8	ns
$t_{su(NSS)}$	NSS setup time	Slave mode	$4t_{PCLK}$	-	ns
$t_{h(NSS)}$	NSS hold time	Slave mode	73	-	ns
$t_{w(SCKH)}$ $t_{w(SCKL)}$	SCK high and low time	Main mode, f_{PCLK} = 36MHz, Prescaler coefficient=4	50	60	ns
$t_{su(MI)}$ $t_{su(SI)}$	Data input setup time	Master mode	5	-	ns
		Slave mode	5	-	
$t_{h(MI)}$ $t_{h(SI)}$	Data input hold time	Master mode	5	-	ns
		Slave mode	3	-	
$t_{a(SO)}$	Data output access time	Slave mode, f_{PCLK} = 20MHz	0	$4t_{PCLK}$	ns
$t_{dis(SO)}$	Data output prohibition time	Slave mode	10		ns

Symbol	Parameter	Conditions	Minimum value	Maximum value	Unit
$t_{v(SO)}$	Effective time of data output	Slave mode (after enable edge)	-	25	ns
$t_{v(MO)}$	Effective time of data output	Master mode (after enable edge)	-	3	ns
$t_{h(SO)}$	Data output hold time	Slave mode (after enable edge)	25	-	ns
$t_{h(MO)}$		Master mode (after enable edge)	4	-	

Note: It is obtained from a comprehensive evaluation and is not tested in production.

Figure 10 SPI Timing Diagram - Slave Mode and CPHA=0

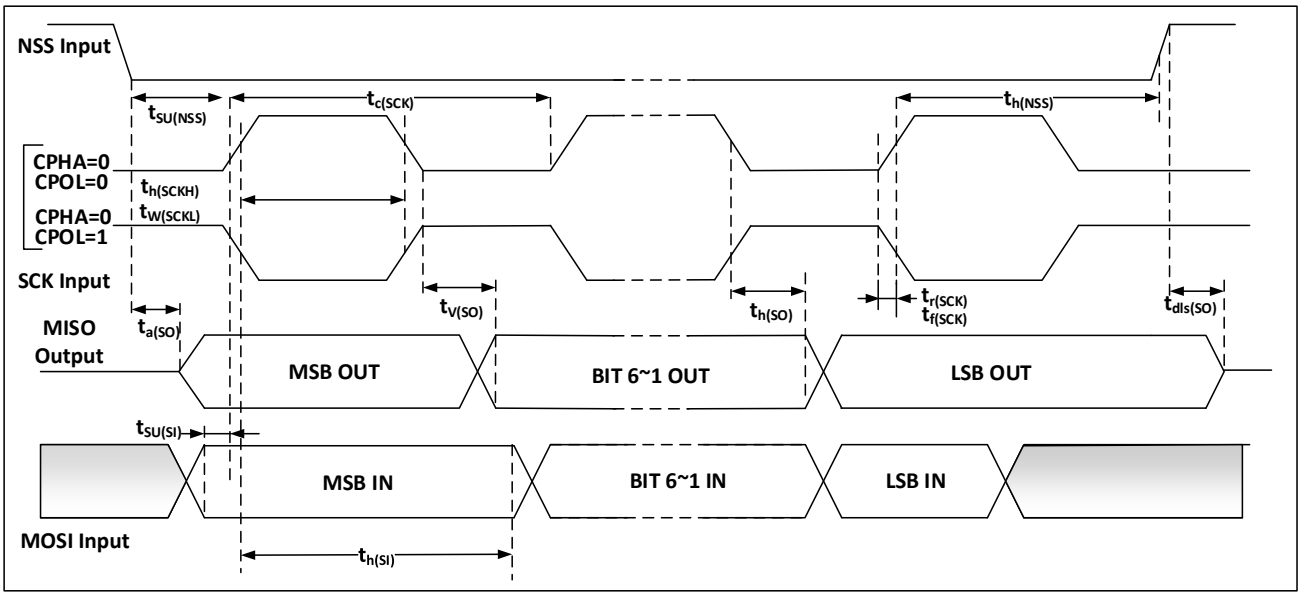
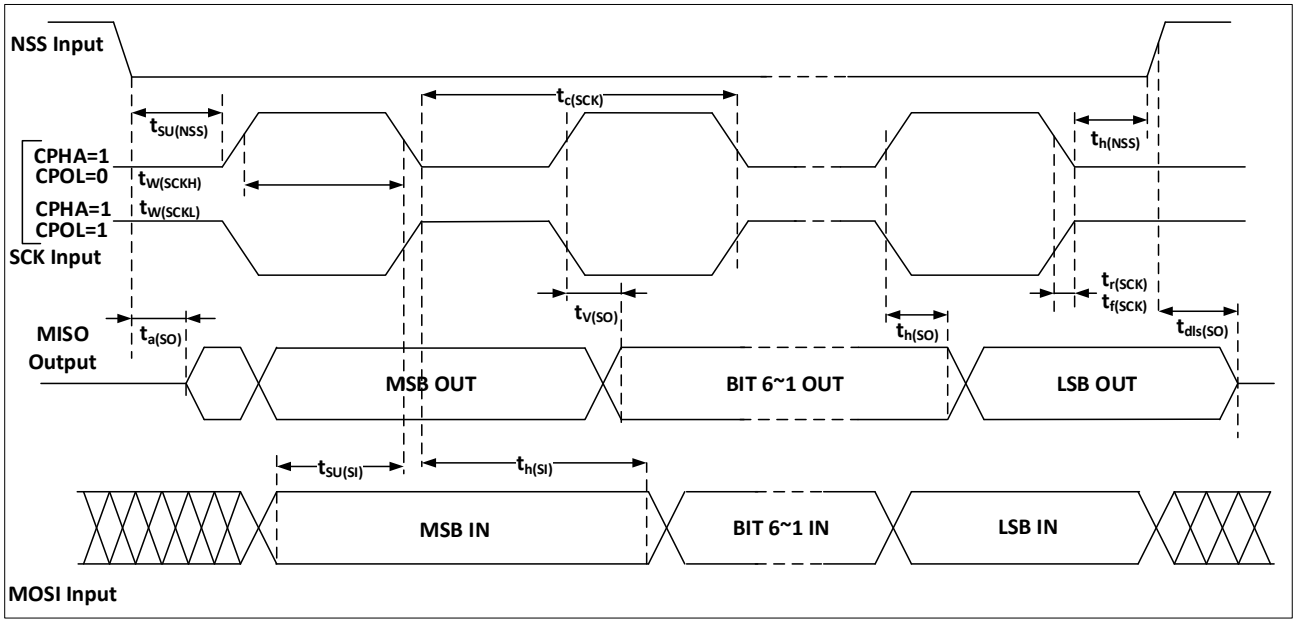
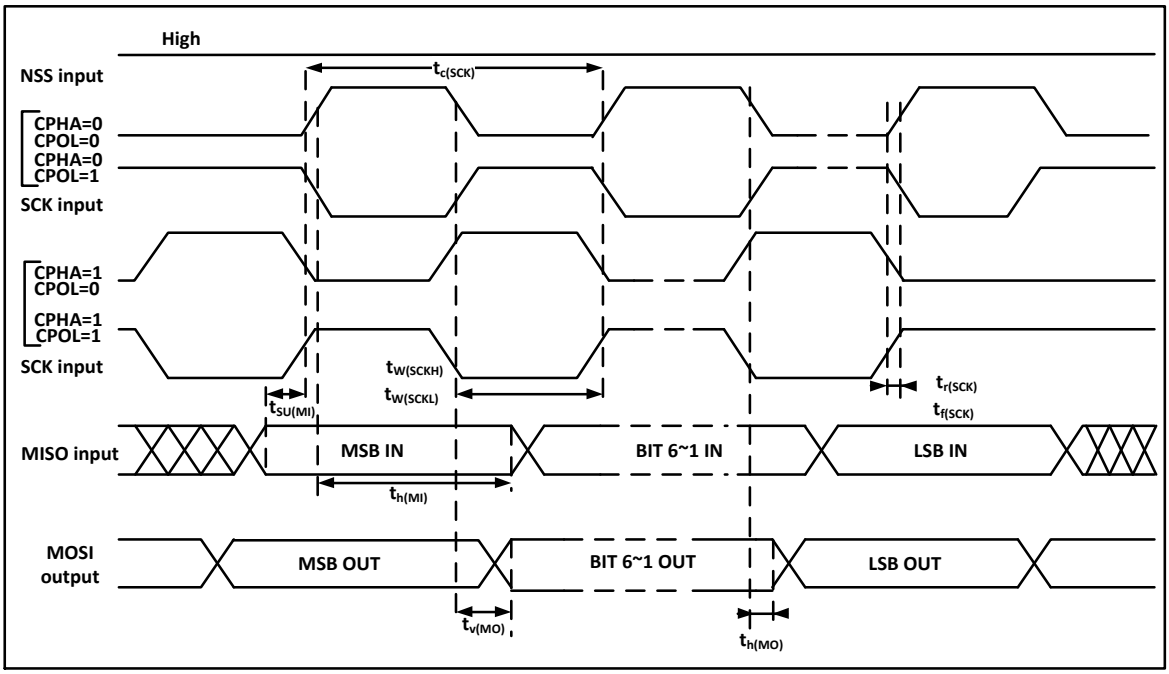


Figure 11 SPI Timing Diagram - Slave Mode and CPHA=1



Note: The measuring points are set at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

Figure 12 SPI Timing Diagram - Master Mode



Note: The measuring points are set at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

5.11. Analog peripherals

5.11.1. ADC

Test parameter description:

- Sampling rate: the number of conversion of analog quantity to digital quantity by ADC per second
- Sample rate=ADC clock/(number of sampling periods + number of conversion periods)

5.11.1.1. 12-bit ADC characteristics

Table 3712-bit ADC Characteristics

Symbol	Parameter	Conditions	Minimum value	Typical values	Maximum value	Unit
V_{DDA}	Power supply voltage	-	2.4	-	3.6	V
I_{DDA}	ADC pwoer consumption	V_{DDA}=3.3V，f_{ADC}=14MHz，Sampling time=1.5 f_{ADC}	-	1	-	mA
f_{ADC}	ADC frequency	-	0.6	-	14	MHz
C_{ADC}	Internal sampling and holding capacitance	-	-	8	-	pF
R_{ADC}	Sampling resistor	-	-	-	1000	Ω
t_S	Sampline Time	f_{ADC}=14MHz	0.107	-	17.1	μs
T_{CONV}	Sampling and conversion time	f_{ADC}=14MHz, 12-bit conversion	1	-	18	μs

Table 3812-bit ADC Accuracy

Symbol	Parameter	Conditions	Typical values	Maximum value	Unit
|ET|	Composite error	f_{PCLK}=56MHz, f_{ADC}=14MHz, V_{DDA}=2.4V-3.6V T_A=-40℃~105℃	-	5	LSB
|EO|	Offset error		-	3	
|EG|	Gain error		-	2.5	
|ED|	Differential linear error		-	3	
|EL|	Integral linear error		-	3	

Note: It is obtained from a comprehensive evaluation and is not tested in production.

5.11.1.2. Test of Built-in Reference Voltage Characteristics

Table 39 Embedded Reference Voltage Characteristics

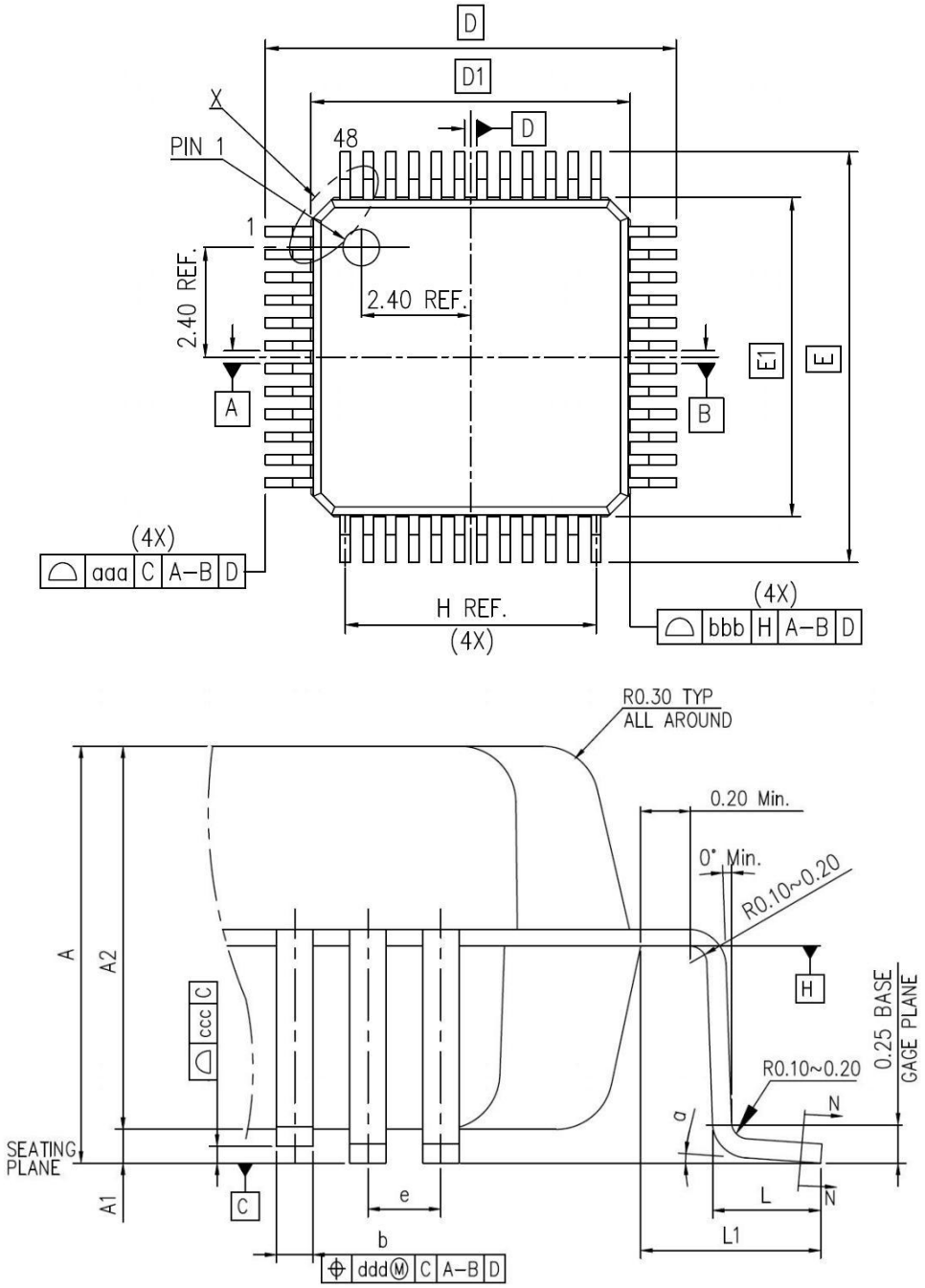
Symbol	Parameter	Conditions	Minimum value	Typical values	Maximum value	Unit
V_{REFINT}	Built-in Reference Voltage	-40℃ < T_A < +105℃ V_{DD}= 2-3.6 V	1.1882	1.1947	1.2002	V
$T_{S\_vrefint}$	Sampling time of ADC when reading out internal reference voltage	-	-	5.1	17.1	μs
V_{RERINT}	Built-in reference voltage extends to temperature range	V_{DD}=3V ±10mV	-	-	18	mV
T_{coeff}	Temperature coefficient	-	-	-	104	ppm/℃

Note: It is obtained from a comprehensive evaluation and is not tested in production.

6. Package information

6.1. LQFP48 Package Diagram

Figure 13 LQFP48 Package Diagram



（1） The figure is not drawn to scale.

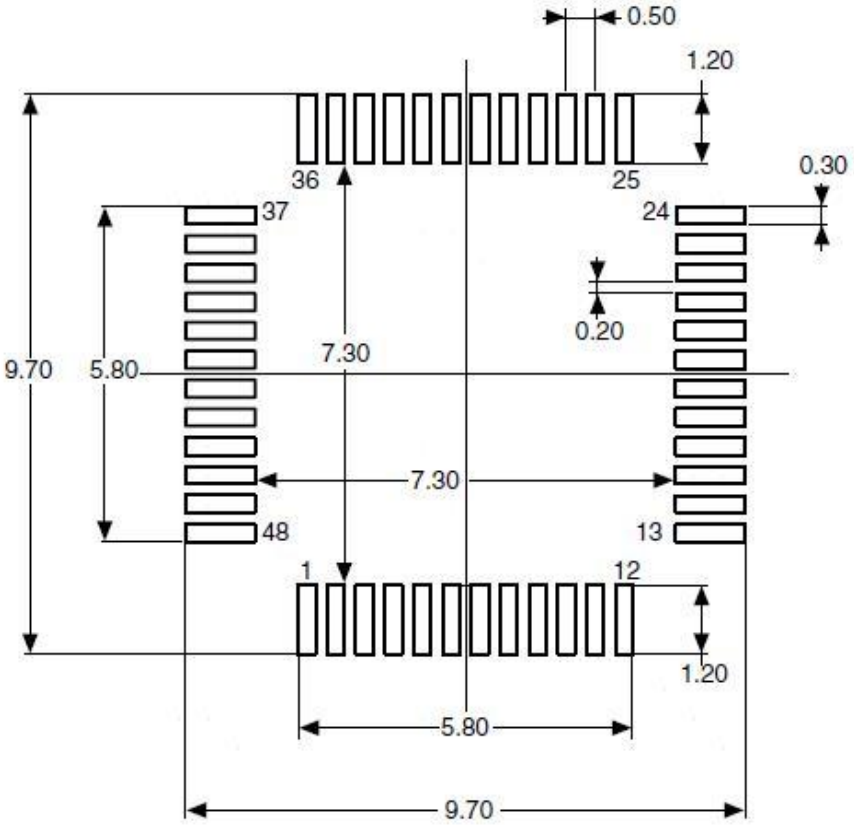
（2） All pins should be soldered to the PCB

Table 40 LQFP48 Package Data

DIMENSION LIST(FOOTPRINT: 2.00)			
S/N	**SYM**	**DIMENSIONS**	**REMARKS**
1	A	MAX. 1.60	OVERALL HEIGHT
2	A1	0.1±0.05	STANDOFF
3	A2	1.40±0.05	PKG THICKNESS
4	D	9.00±0.20	LEAD TIP TO TIP
5	D1	7.00±0.10	PKG LENGTH
6	E	9.00±0.20	LEAD TIP TO TIP
7	E1	7.00±0.10	PKG WDTH
8	L	0.60±0.15	FOOT LENGTH
9	L1	1.00 REF	LEAD LENGTH
10	T	0.15	LEAD THICKNESS
11	T1	0.127±0.03	LEAD BASE METAL THICKNESS
12	a	0°~7°	FOOT ANGLE
13	b	0.22±0.02	LEAD WIDTH
14	b1	0.20±0.03	LEAD BASE METAL WIDTH
15	e	0.50 BASE	LEAD PITCH
16	H(REF.)	(5.50)	CUM. LEAD PITCH
17	aaa	0.2	PROFILE OF LEAD TIPS
18	bbb	0.2	PROFILE OF MOLD SURFACE
19	ccc	0.08	FOOT COPLANARITY
20	ddd	0.08	FOOT POSITION

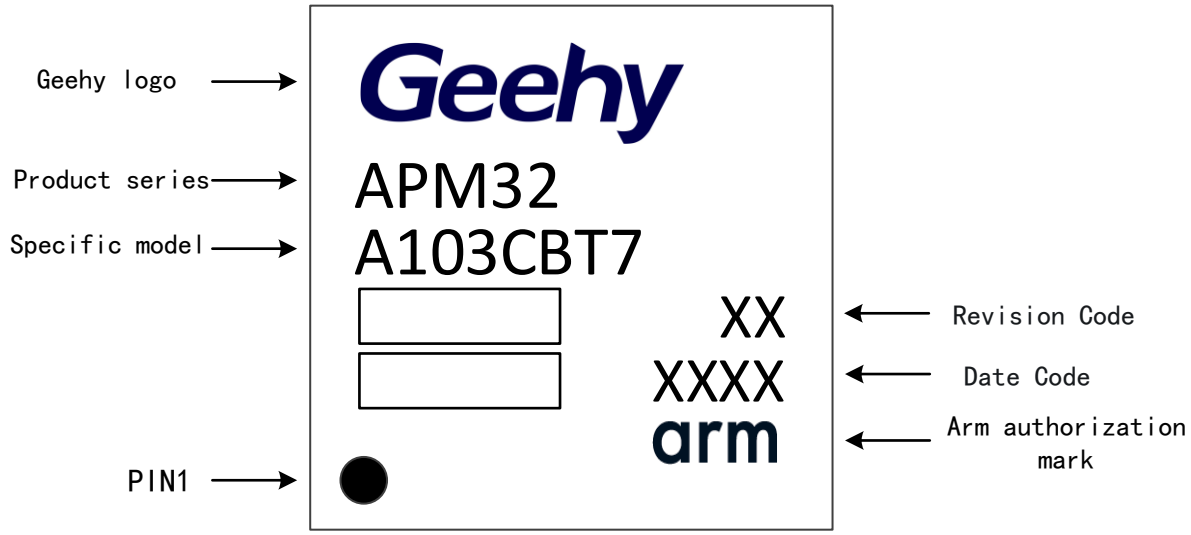
（1） Dimensions are expressed in mm

Figure 14 LQFP48 recommended welding Layout



（1） Dimensions are expressed in mm

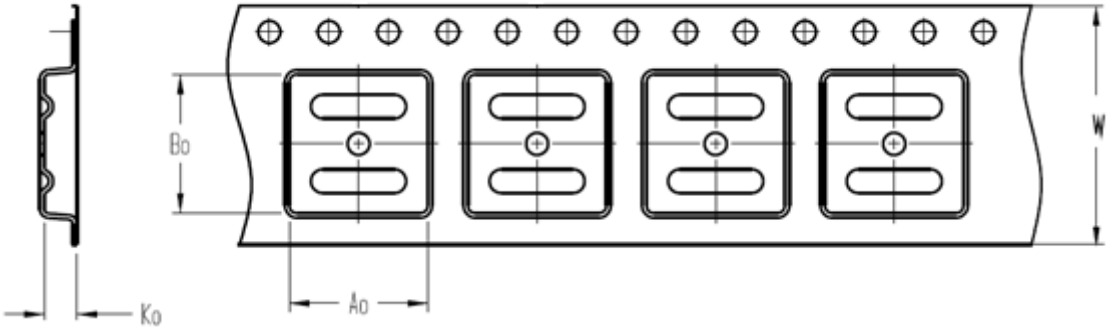
Figure 15 LQFP48 pins identification diagram



7. Packaging information

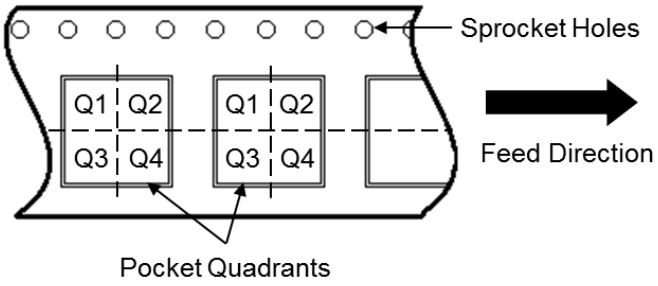
7.1. Reel packaging

Figure 16 Specification Drawing of Reel Packaging

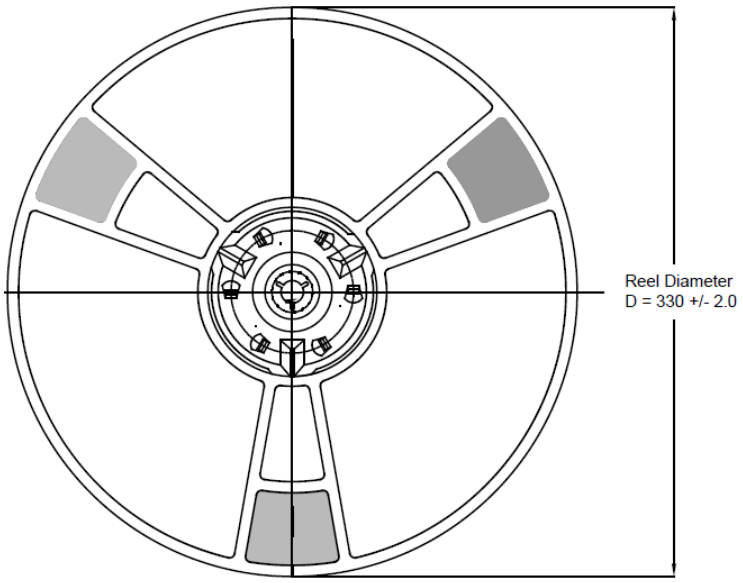


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape

Quadrant Assignments for PIN1 Orientation in Tape



Reel Dimensions



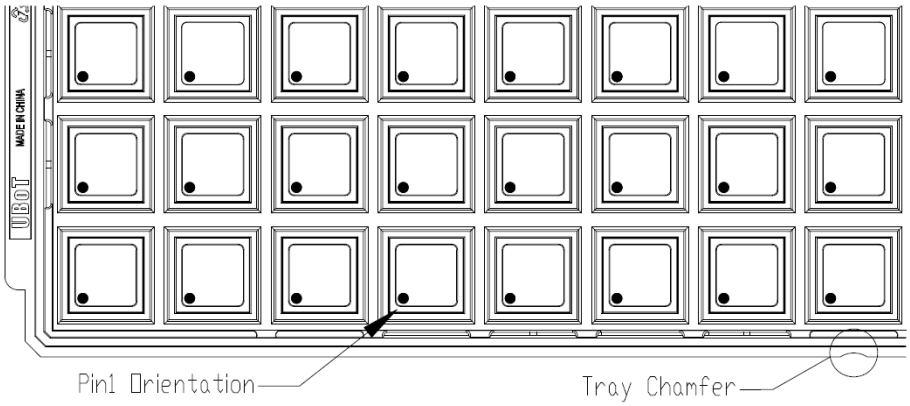
All photos are for reference only, and the appearance is subject to the product.

Table 41 Reel Packaging Parameter Specification Table

Device	Package Type	Pins	SPQ	Reel Diameter (mm)	A0 (mm)	B0 (mm)	K0 (mm)	W (mm)	Pin1 Quadrant
APM32A103CBT7	LQFP	48	2000	330	9.3	9.3	2.2	16	Q1

7.2. Tray packaging

Figure 17 Tray Packaging Diagram



Tray Dimensions

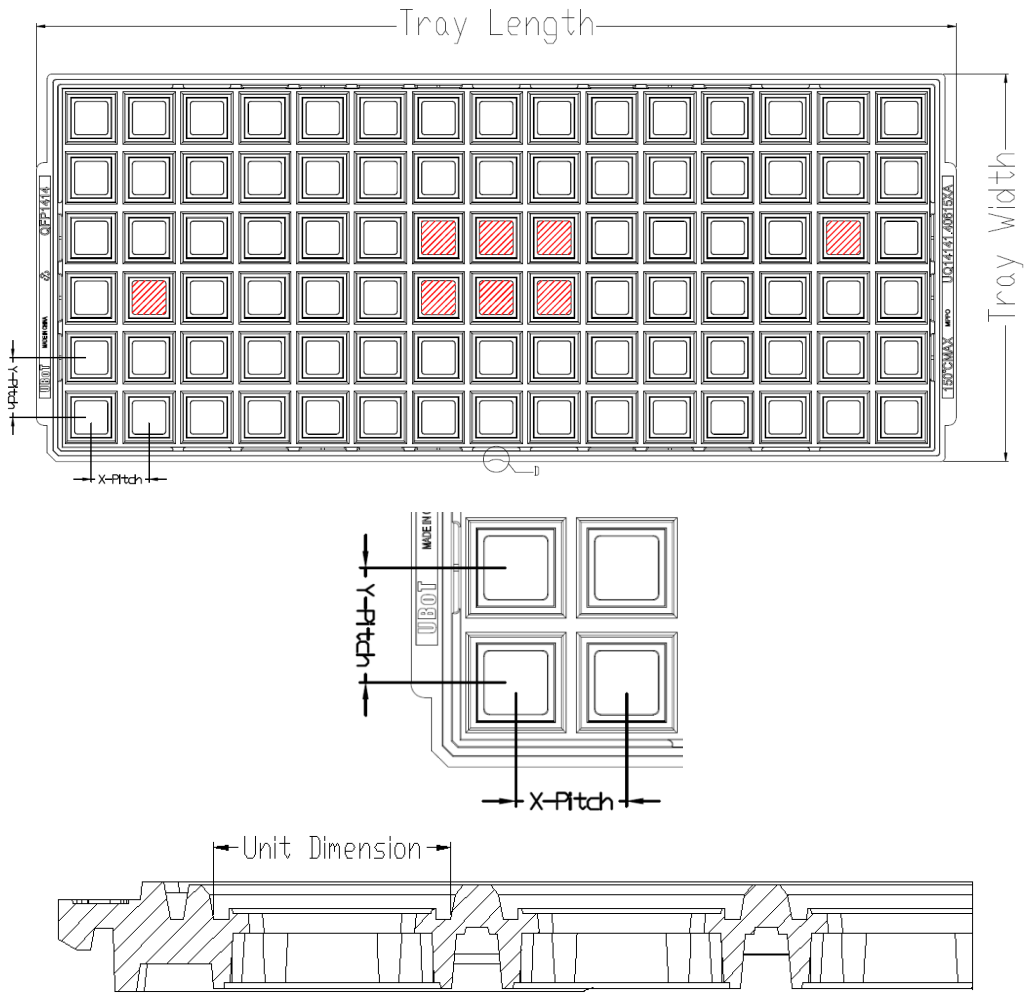


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Table 42 Tray Packaging Parameter Specification Table

Device	Package Type	Pins	SPQ	X-Dimension（mm）	Y-Dimension（mm）	X-Pitch（mm）	Y-Pitch（mm）	Tray Length（mm）	Tray Width（mm）
APM32A103CBT7	LQFP	48	2500	9.7	9.7	12.2	12.6	322.6	135.9

8. Ordering information

Figure 18 Product Naming Rules

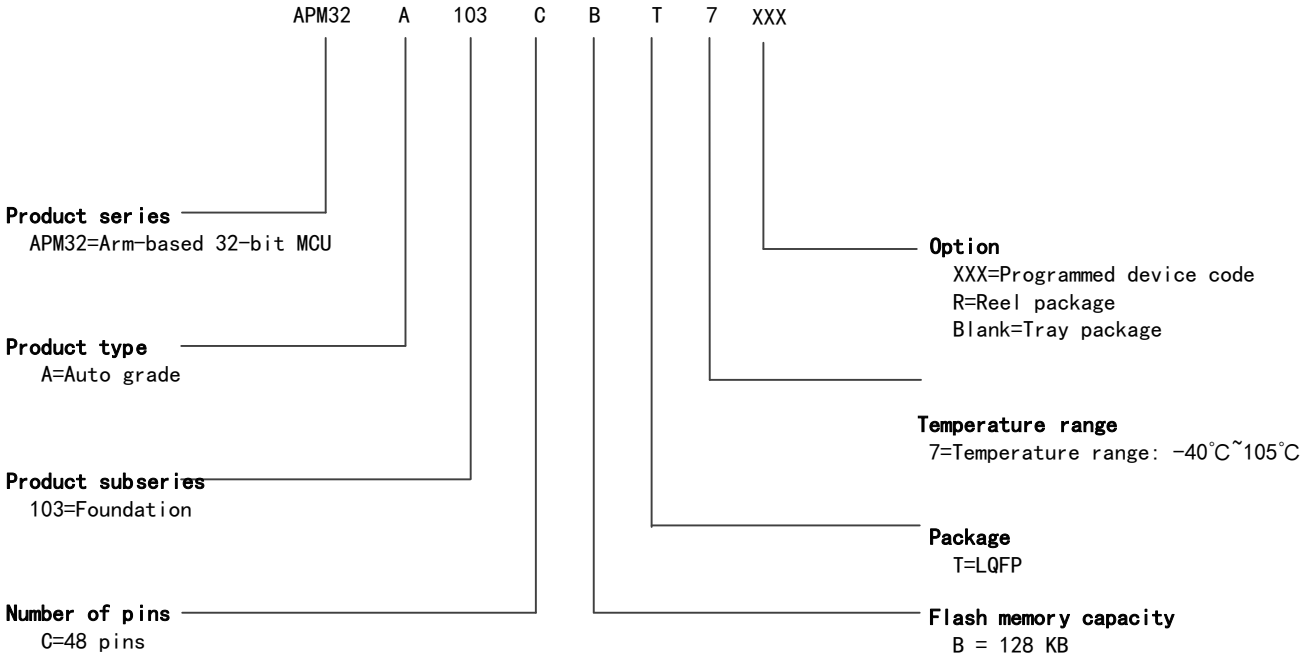

Table 43 Ordering Information Table

Order Code	Flash (KB)	SRAM (KB)	Package	SPQ	Temperature Range
APM32A103CBT7	128	20	LQFP48	2500	-40℃~105℃
APM32A103CBT7-R	128	20	LQFP48	2000	-40℃~105℃

Note: SPQ=Smallest Packaging Quantity

9. Commonly used function module denomination

Table 44 Commonly Used Function Module Denomination

Chinese description	Short name
Reset management unit	RMU
Clock management unit	CMU
Reset and clock management	RCM
External interrupt	EINT
Genera-purpose IO	GPIO
Multiplexing IO	AFIO
Wake up controller	WUPT
Independent watchdog timer	IWDT
Window watchdog timer	WWDT
Timer	TMR
CRC controller	CRC
Power Management Unit	PMU
DMA controller	DMA
Analog-to-digital converter	ADC
Real-time clock	RTC
External memory controller	EMMC
Controller local area network	CAN
I2C interface	I2C
Serial peripheral interface	SPI
Universal asynchronous transmitter receiver	UART
Universal synchronous and asynchronous transmitter receiver	USART
Flash interface control unit	FMC

10. Revision history

Table 1 Document Revision History

Date	Version	Change History
December 2022	1.0	New
August 2024	1.1	(1) Modify the describtion of address mapping (2) Add automotive class descriptions
August 2025	1.2	Remove ADC Tsensor descriptions

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